

PRAHA EXT GFX

CPU : Intel Merom (800MHz)
Chip Set : RS600ME & SB600
Remarks : Mobility Platform

Model Name : PRAHA EXT GFX
PBA Name : MAIN
PCB Code : NANYA:BA41-00806A
GCE : BA41-00812A
TPT : BA41-00814A
Dev. Step : PR2 (8-Layer)
Revision : 1.0
T.R. Date : 2007.06.24

DRAW	CHECK	APPROVAL

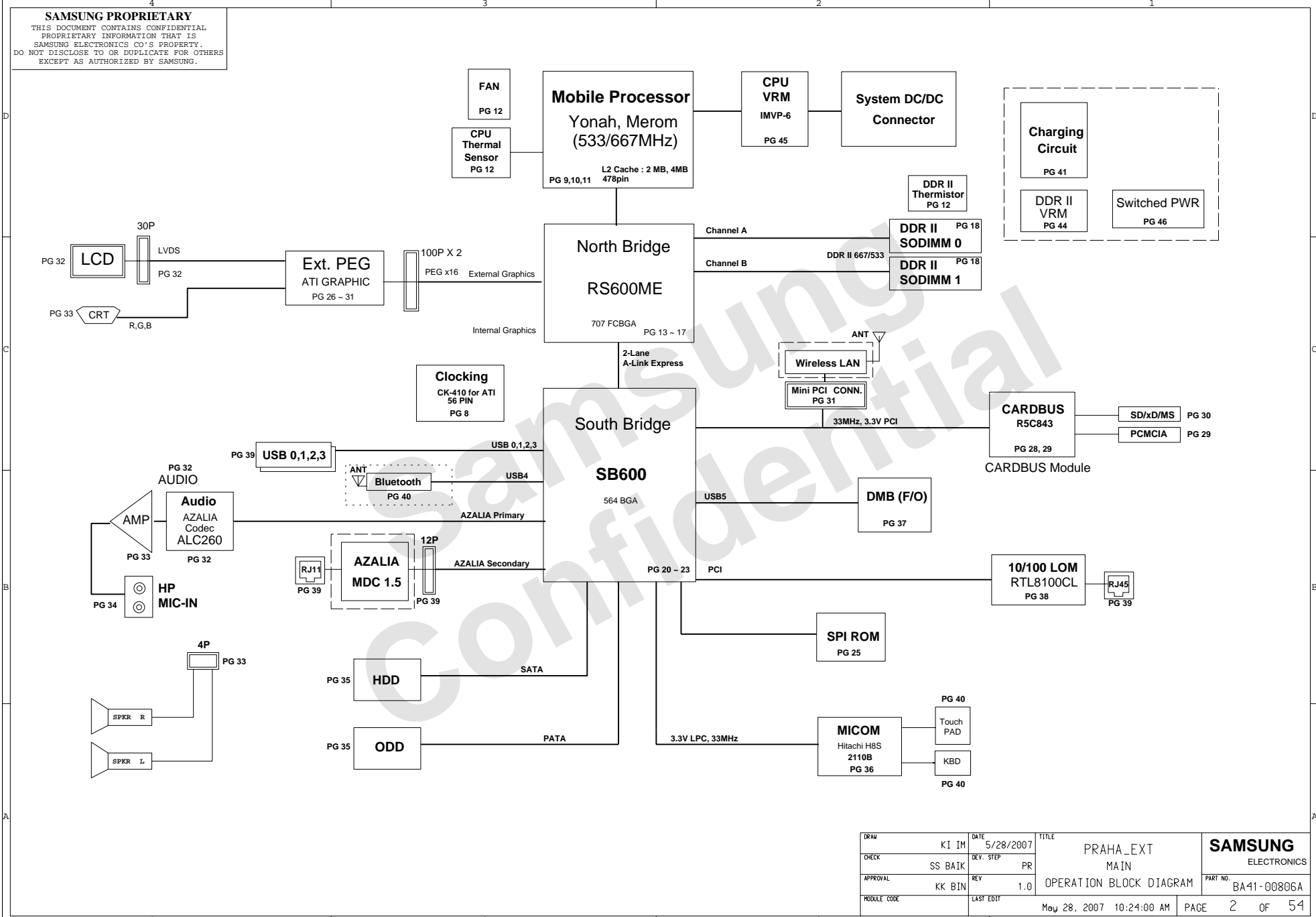
Owner : SEC Mobile R & D Signature : X

Table of Contents

Sheet 1. COVER
Sheet 2-6. DIAGRAM (Block/Power) & ANNOTATIONS
Sheet 7. CLOCK GENERATOR
Sheet 8-10. YONAH
Sheet 11. THERMAL SENSOR / FAN CONTROL
Sheet 12-16. RS600ME
Sheet 17. DDR II SODIMM
Sheet 18. DDR II TERMINATION
Sheet 19-22. SB600
Sheet 23. SB600 STRAPS
Sheet 24. SPI ROM & DEBUG CARD CONN
Sheet 26-30. ATI M64S VIDEO CHIP
Sheet 31. LCD
Sheet 32. CRT
Sheet 33. EXPRESS CARD
Sheet 34. 2 IN 1
Sheet 35. MINICARD
Sheet 36-38. AUDIO
Sheet 39. HDD(SATA) & ODD(IDE)
Sheet 40. MICOM
Sheet 41. LOM WITH COMBO JACK
Sheet 42. USB & MDC
Sheet 43. LED & BLUETOOTH & TOUCHPAD & KEYBOARD & LID S/W
Sheet 44. CHARGER
Sheet 45. P3.3V_AUX & P5.0V_AUX
Sheet 46. P1.2V & P1.2V_AUX & VCCP
Sheet 47. DDR2 POWER
Sheet 48. EXTERNAL GFX_POWER
Sheet 49. CPU VRM
Sheet 50. P1.5V POWER & SWITCHED POWER & MICOM RESET
Sheet 50. ICT PORT
Sheet 51. P1.2V_NB / P2.5V POWER
Sheet 52. DISCHARGE & MOUNT HOLE
Sheet 53. EMI FINGER / ICT CAPACITOR
Sheet 54. TP

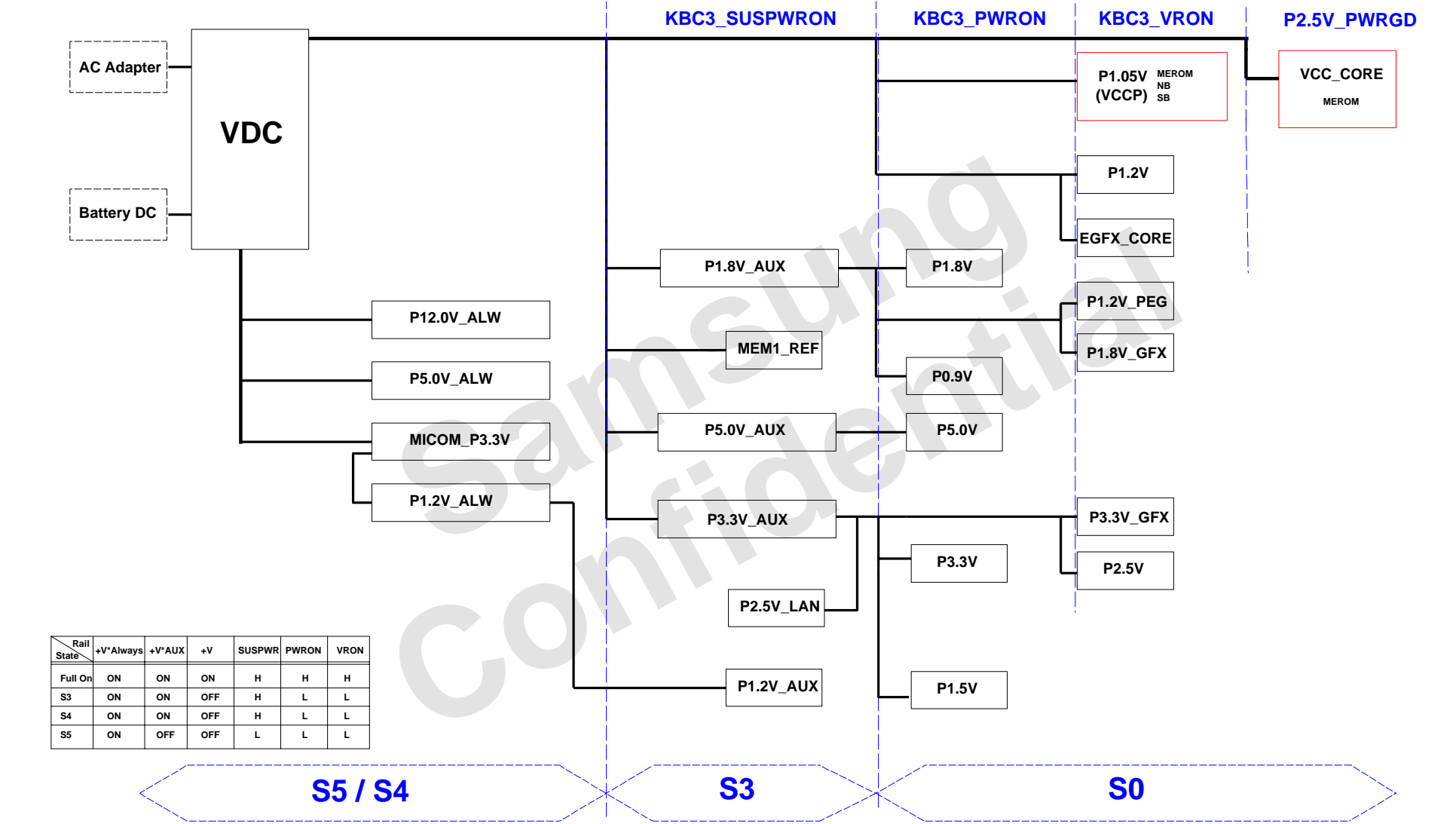
USE ICT PORT

DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG
CHECK	SS BAIK	DEV. STEP	PR		COVER	ELECTRONICS
APPROVAL	KK BIN	REV	1.0			PART NO. BA41-00806A
MODULE CODE		LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	1	OF 54

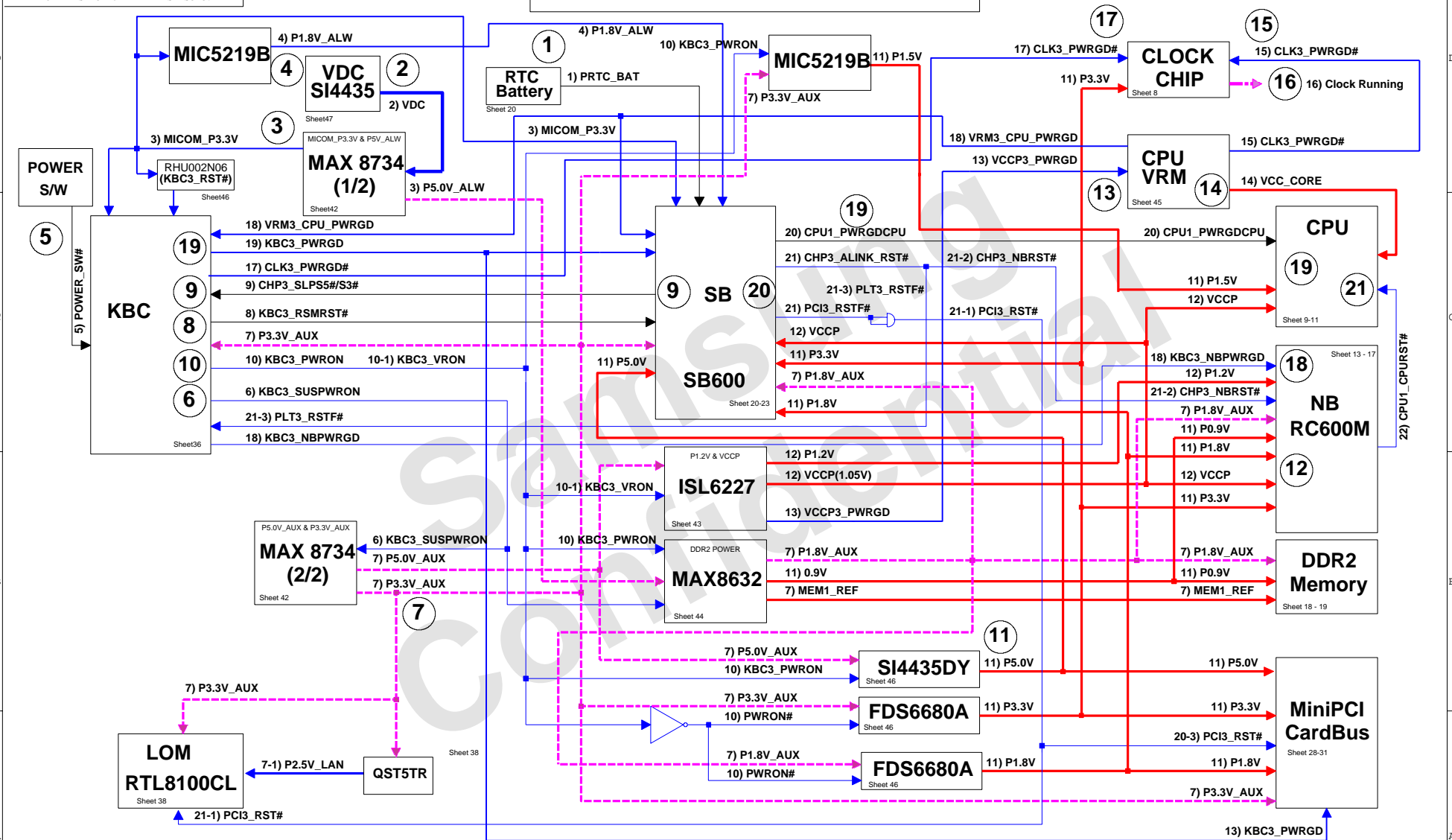


DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG
CHECK	SS BAIK	DEV. STEP	PR	MAIN	OPERATION BLOCK DIAGRAM	ELECTRONICS
APPROVAL	KK BIN	REV	1.0			PART NO. BA41-00806A
MODULE CODE		LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	2	OF 54

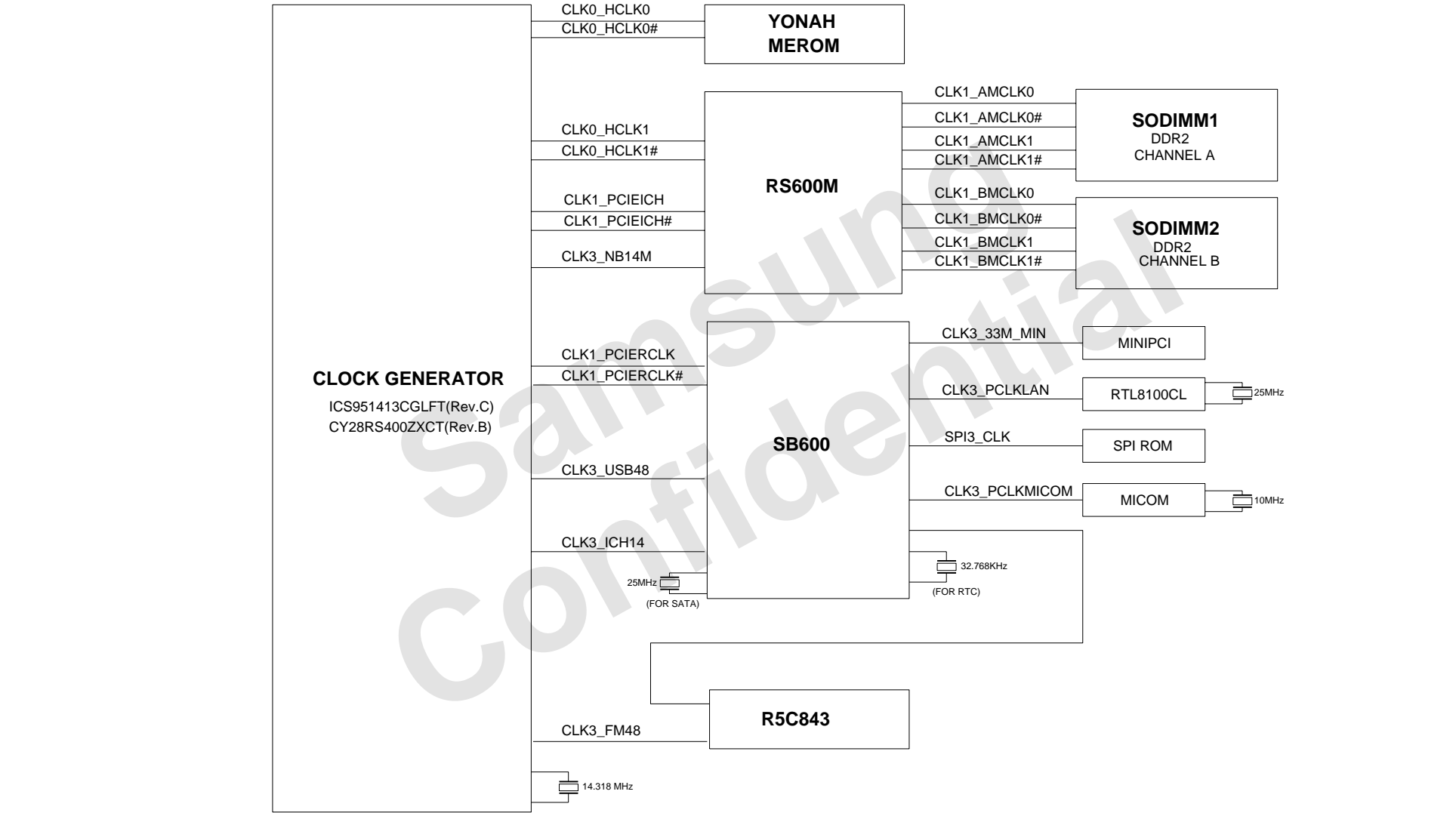
Power Diagram



POWER SEQUENCE Rev. 0.1



DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG
CHECK	SS BAIK	DEV. STEP	PR			ELECTRONICS
APPROVAL	KK BIN	REV	1.0	POWER SEQUENCE		PART NO. BA41-00806A
MODULE CODE		LAST EDIT		May 28, 2007 10:24:00 AM	PAGE 4	OF 54



DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR			
APPROVAL	KK BIN	REV	1.0			PART NO. BA41-00806A
MODULE CODE		LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	5 OF 54	

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A, B, C
LAN	AD21	1	D
MINIPCI	AD23	2	A,B
USB	AD30(internal)	-	-
Hub to PCI	AD31(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	--
Internal MAC	AD31(internal)	-	-
AC Link	-	-	-

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for YONAH (0-1.5V)
VCCP	YONAH Processor System Bus(PSB) Termination (1.05V)
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P1.8V_ALWS	1.8V power rail (Always On)
P2.5V_LAN	2.5V power rail (off in S4-S5)
MICOM_P3.3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P5.0V_ALWS	5.0V power rail (Always On)
P12V_ALWS	12V power rail (Always On)

I²C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
SODIMM0	1010 0100	A4h	-
SODIMM1	1010 0110	A6h	-
CK-410 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0, 1	SYSTEM PORT A
2, 3	SYSTEM PORT B
4	BLUETOOTH
5	DMB

System Power States

- CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.
- CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

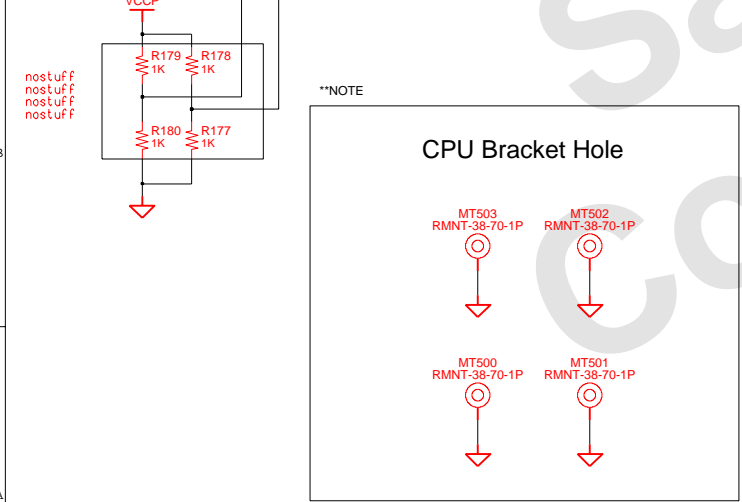
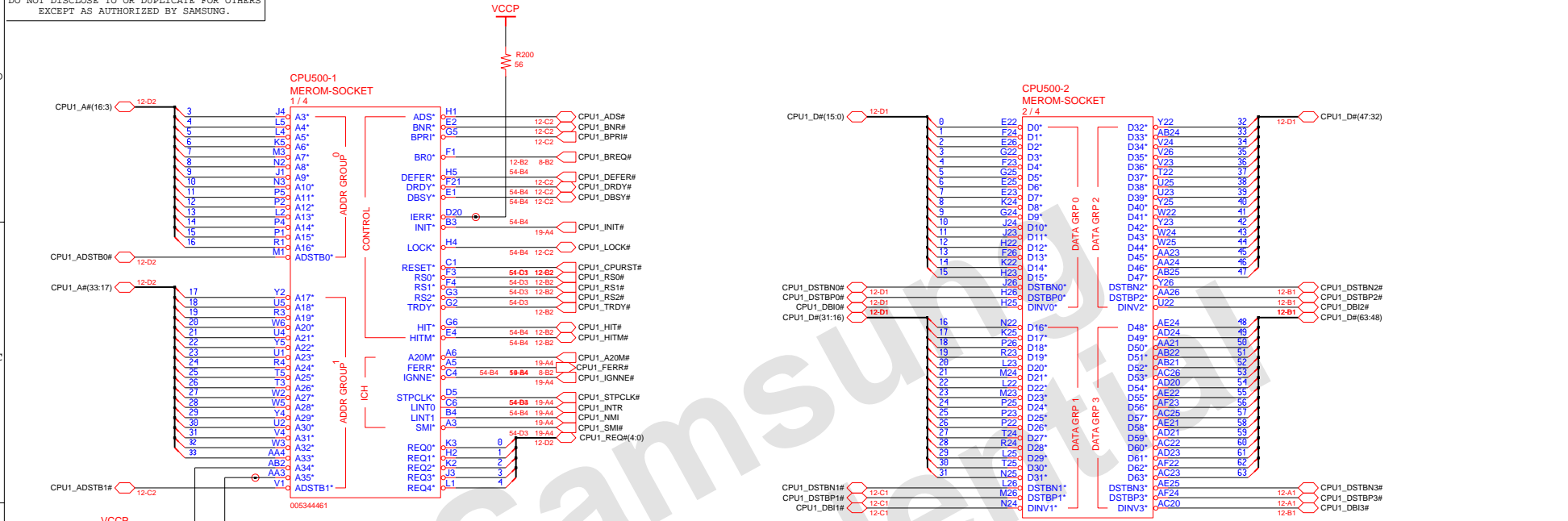
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB600	Real Time Clock
Crystal	25MHz	SB600	SATA
Crystal	10MHz	MICOM	HBS-2110B
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	25MHz	LAN	LOM

CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 0	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 0 1	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 0 1	0.9750 V	1 0 1 0 0 1 0	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 1 0 0 0	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 1	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 1 0	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 1	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 1 0 0	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 1	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 1 0	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 1	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 1 0 0 0 0	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 1	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 1 0	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 1	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 1 0 0	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 1	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 1 0	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 1	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 1 0 0 0	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 1	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 1 0	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 1	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 1 0 0	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 1	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 1 0	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 1	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 0 1 1 1	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 0 1 0 0	0.5875 V	1 1 1 0 0 0 1	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 0 1 0 1	0.5750 V	1 1 1 0 0 1 0	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 0 1 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 0 1 1 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 0 1 1 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 0 1 1 1	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 0 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 0 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG
CHECK	SS BAIK	DEV. STEP	PR		MAIN	ELECTRONICS
APPROVAL	KK BIN	REV	1.0		BOARD INFORMATION	PART NO. BA41-00806A
MODULE CODE		LAST EDIT			May 28, 2007 10:24:00 AM	PAGE 6 OF 54



DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT MAIN MEROM CPU (1/3)	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR			PART NO. BA41-00806A
APPROVAL	KK BIN	REV	1.0			
MODULE CODE		LAST EDIT				

May 28, 2007 10:24:00 AM

PAGE 8 OF 54

IMVP-6



*Yonah Processor (2.33 GHz / 800 MHz : TBD)

VCCI

d:/users/mobile20/mentor/praha/pr/praha_main-ex

The diagram illustrates the VCC_CORE power plane layout. It features a top rail connected to VCC_CORE and a bottom rail connected to ground. A series of decoupling capacitors (C284 to C287) are placed along the top rail, each with a 20% tolerance. Sense points for CPU1_VCCSENSE and CPU1_VSSSENSE are indicated with resistors R175 and R174, respectively, connected to the top and bottom rails. A series of decoupling capacitors (C320 to C309) are placed along the bottom rail, with values ranging from 22000nF to 22000nF, and some labeled as 'not used'.

VCCP

EC13
330µF
2.5V
OXI

C299
100nF
10V

C298
100nF
10V

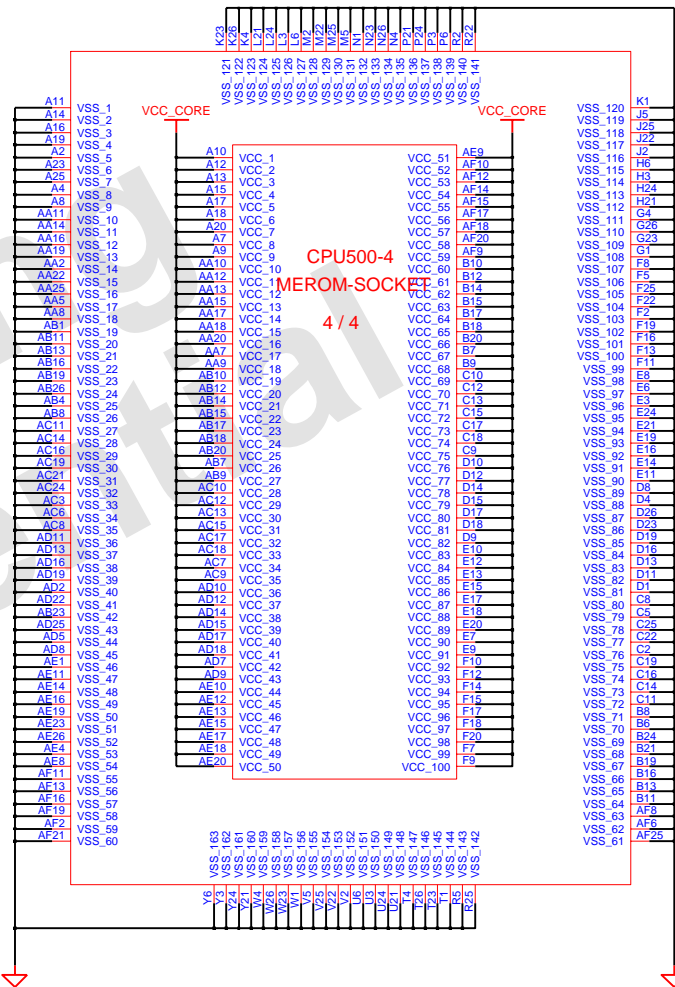
C289
100nF
10V

C297
100nF
10V

C290
100nF
10V

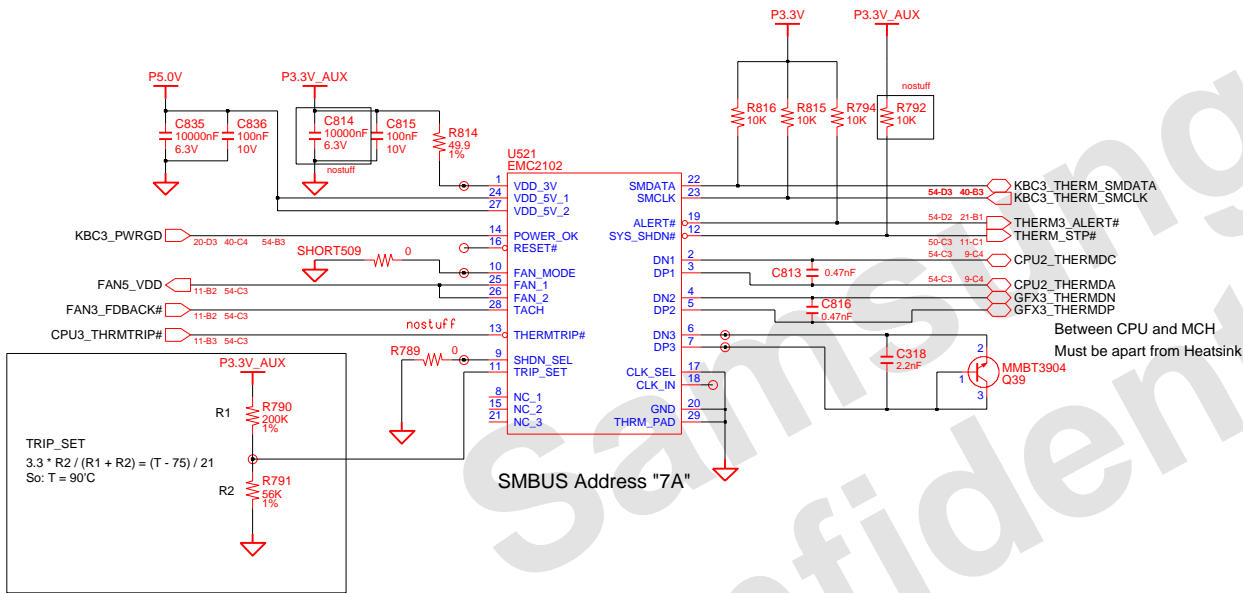
C288
100nF
10V

notstiff



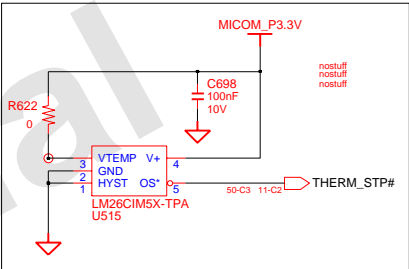
DRAW	KI IM	DATE	5/28/2007	TITLE		SAMSUNG ELECTRONICS	
CHECK	SS BAIK	DEV. STEP	PR				
APPROVAL	KK BIN	REV	1.0				
MODULE CODE		LAST EDIT		May 28, 2007 10:24:00 AM	PAGE	10	OF 54

Thermal Monitor

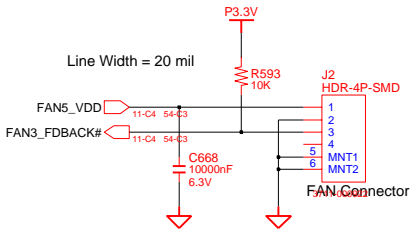
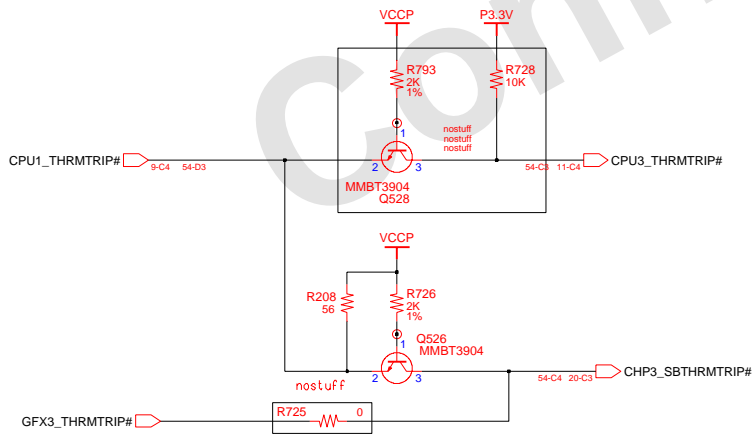


- Refer To Thermal Sensor Layout Guidelines.
- Place the Thermal Sensor close to a remote diode.
 - Keep traces away from high voltage (+12V bus)
 - Keep traces away from fast data buses and CRT signal.
 - Use recommended trace widths and spacings (10mil)
 - Place a ground plane under the traces.
 - Use guard traces flanking DXP and DXN and connecting to GND

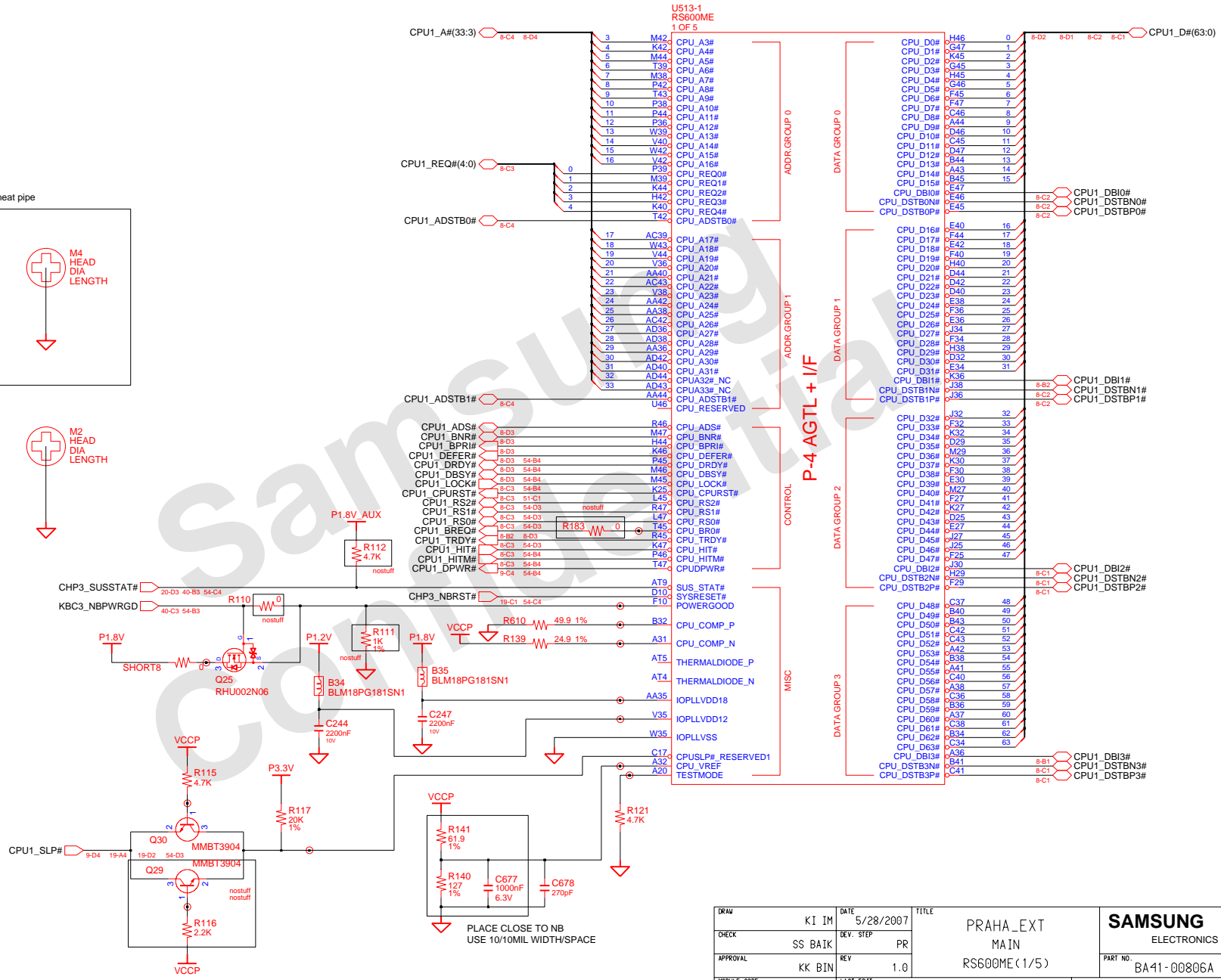
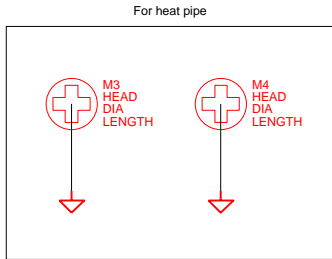
OTP (NOSTUFF)



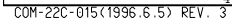
FAN Control

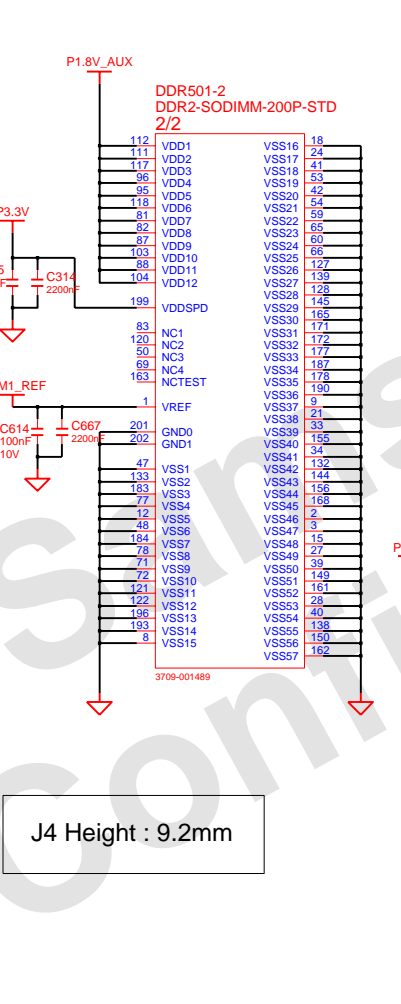
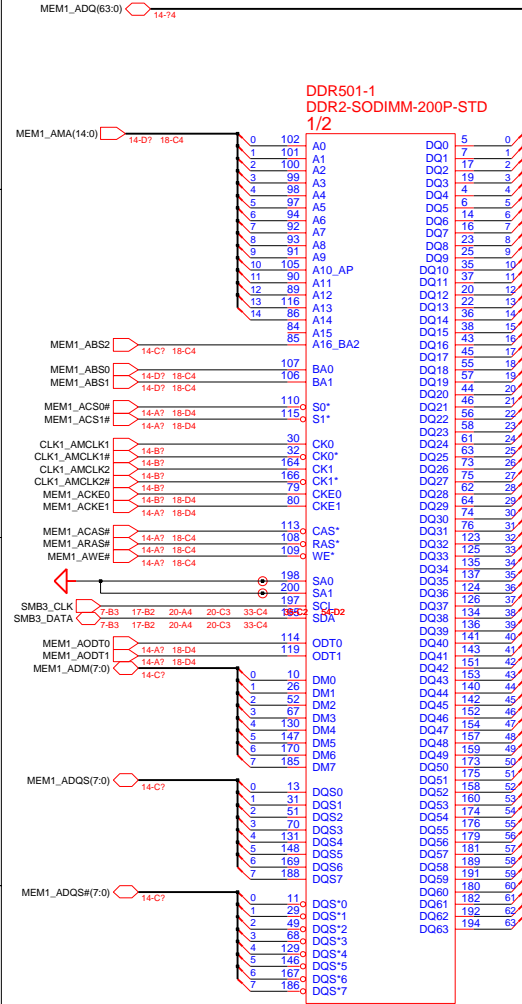


DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR		MAIN	
APPROVAL	KK BIN	REV	1.0		THERMAL SENSOR/FAN CNTRL	
MODULE CODE		LAST EDIT				
				May 28, 2007 10:24:00 AM	PAGE 11 OF 54	PART NO. BA41-00806A

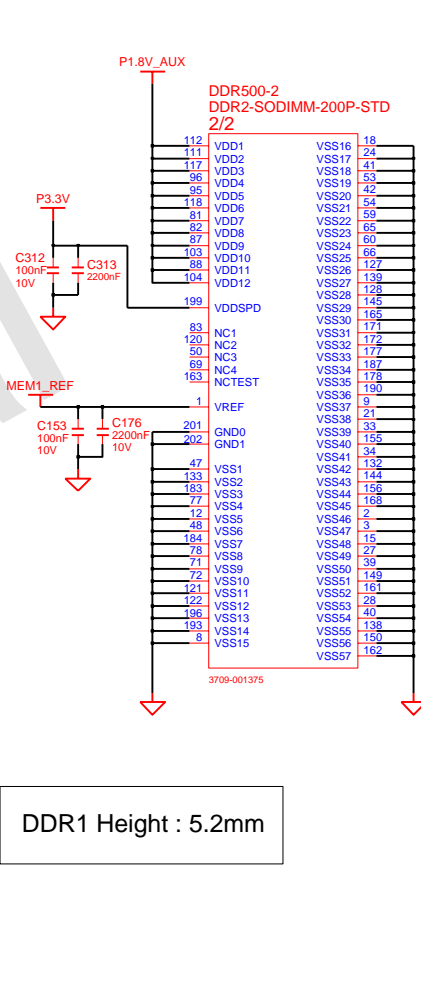
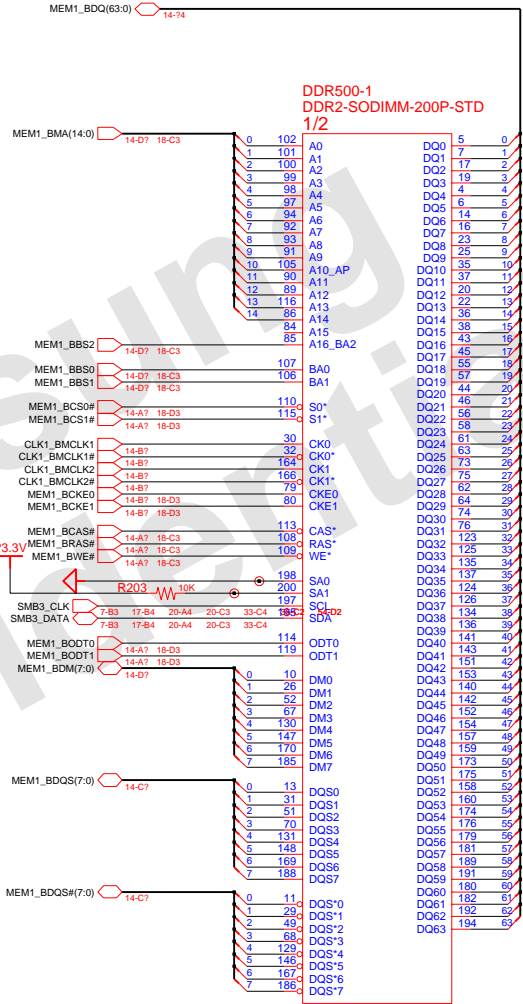






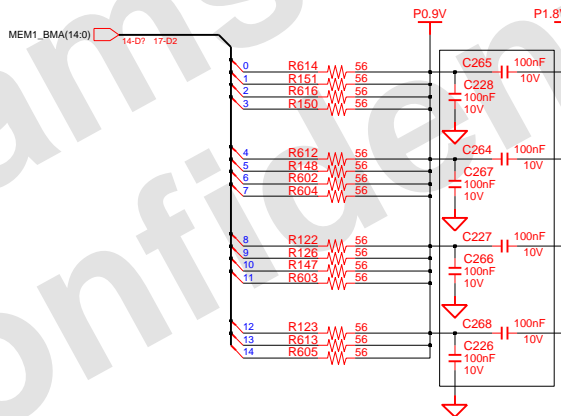
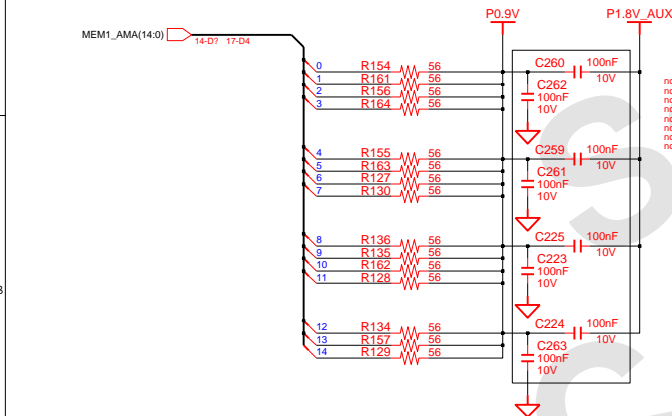
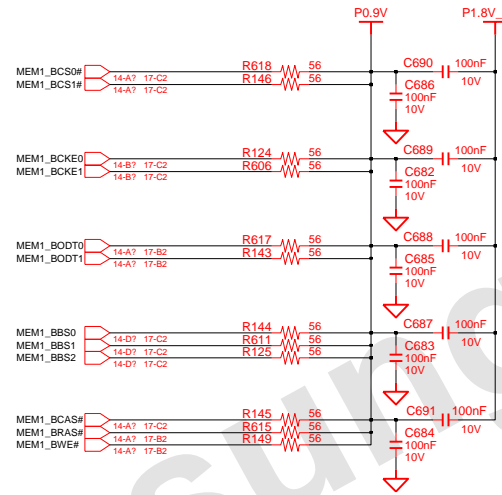
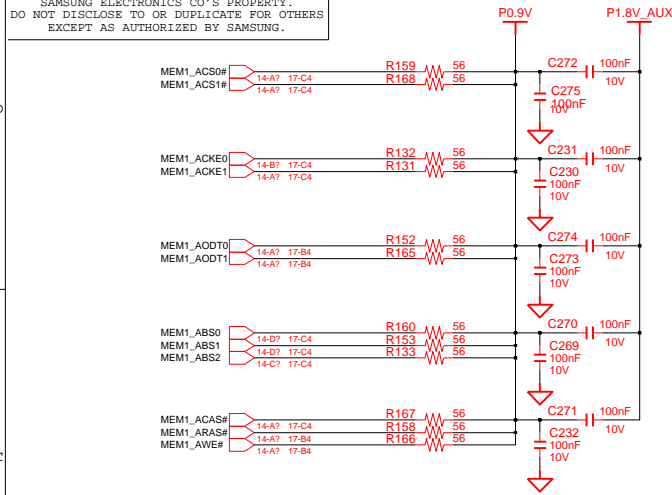


J4 Height : 9.2mm

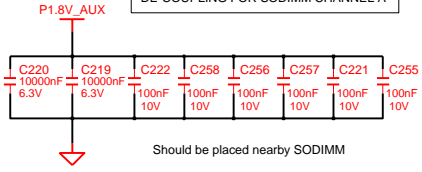


DDR1 Height : 5.2mm

DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG
CHECK	SS BAIK	DEV. STEP	PR		MAIN	ELECTRONICS
APPROVAL	KK BIN	REV	1.0		DDR2 - SODIMM	PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT		May 28, 2007 10:24:00 AM	PAGE 17	OF 54

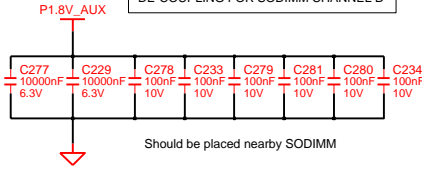


DE-COUPLING FOR SODIMM CHANNEL A



Should be placed nearby SODIMM

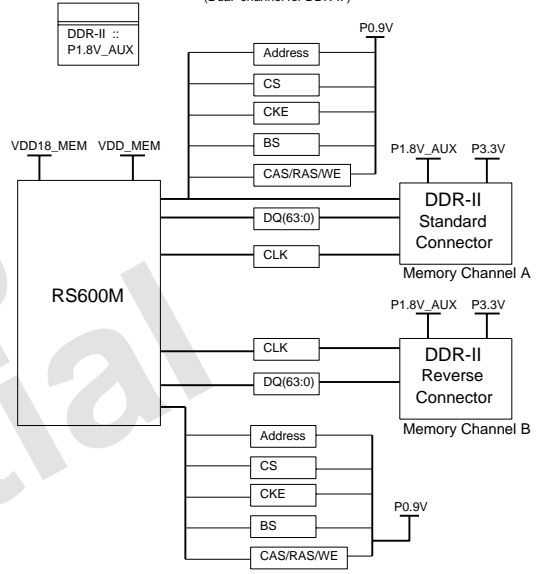
DE-COUPLING FOR SODIMM CHANNEL B



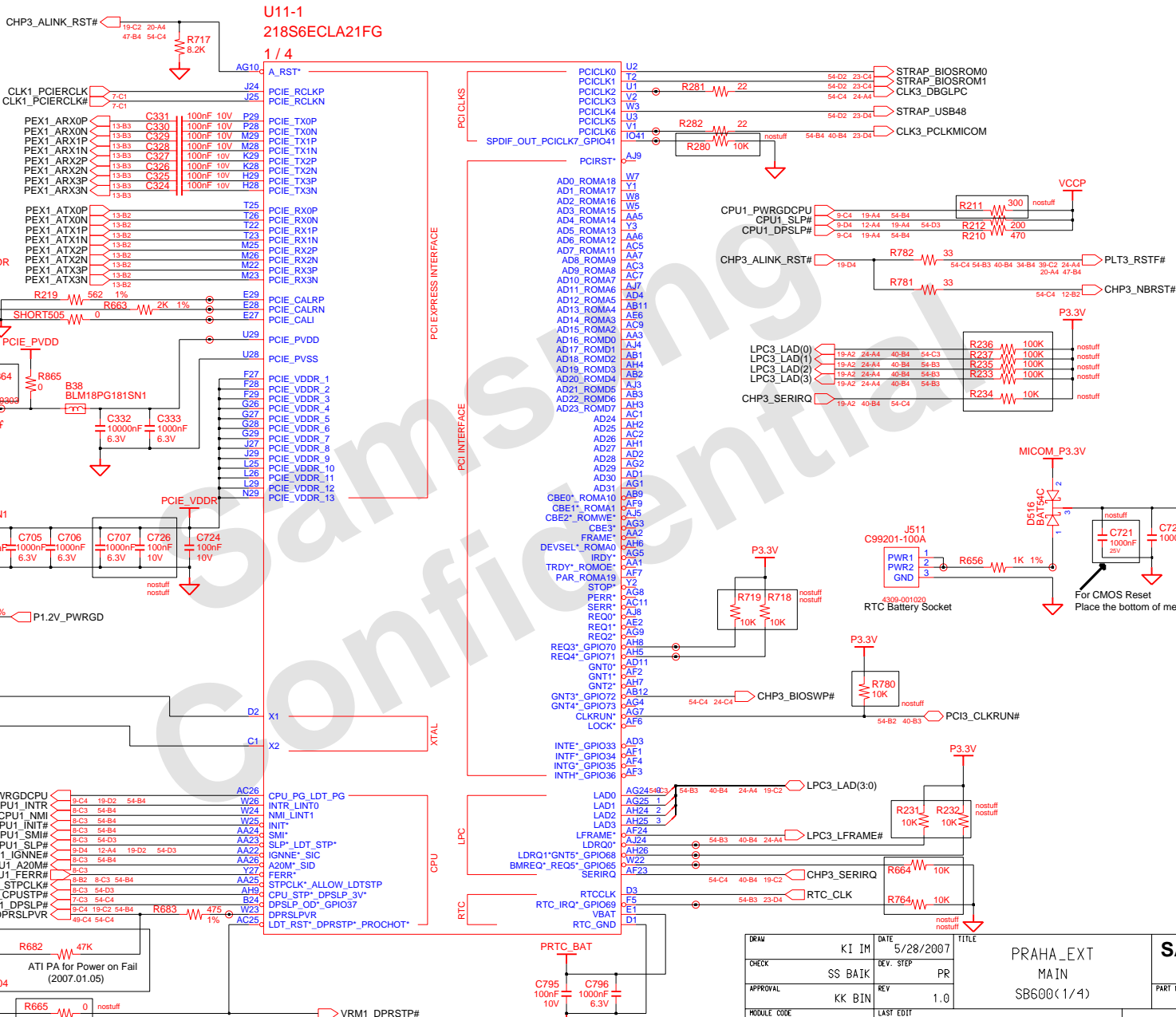
Should be placed nearby SODIMM

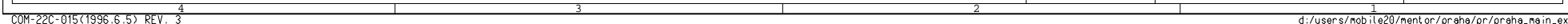
Memory Topology

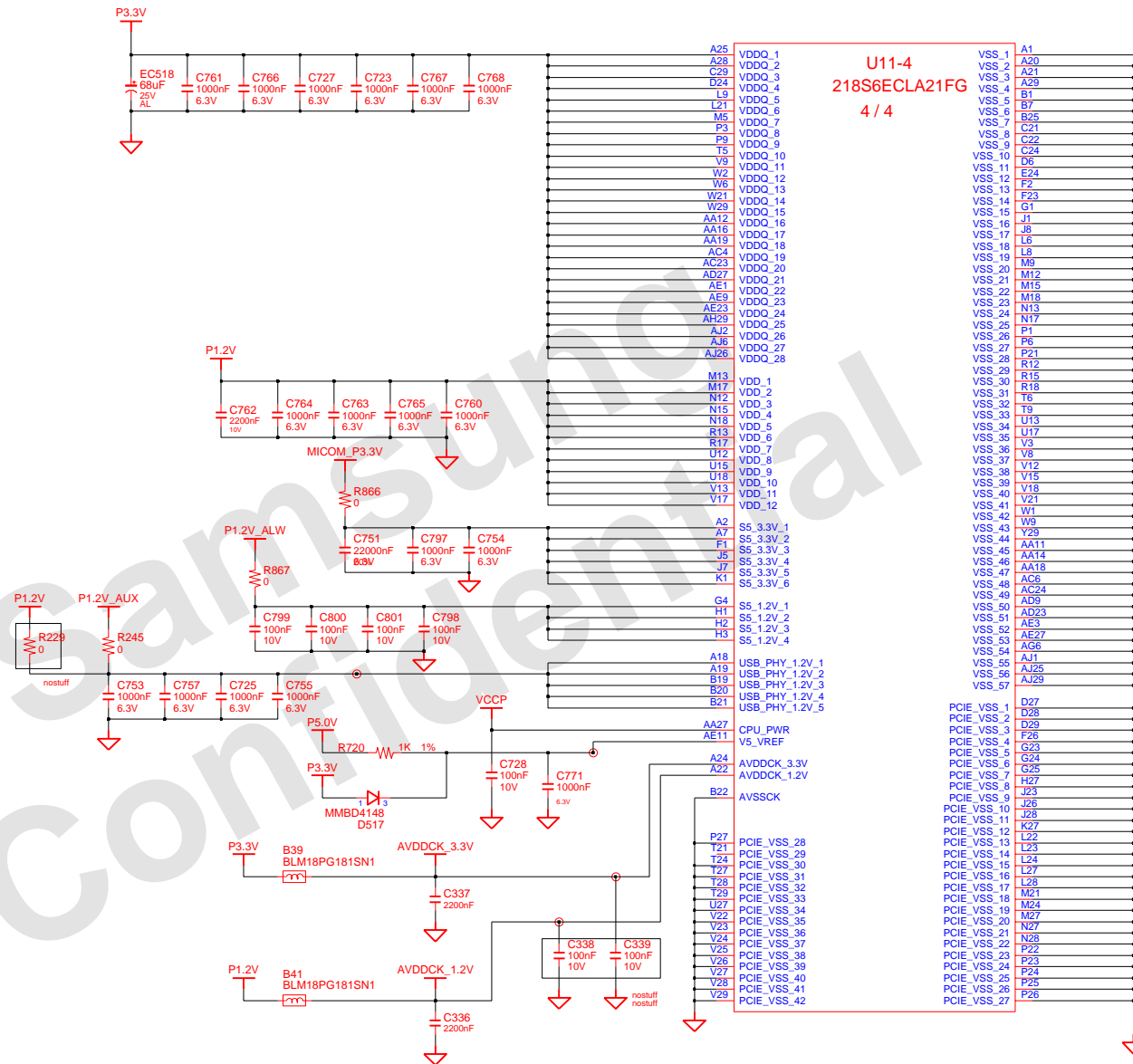
(Dual channel for DDR-II)



DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT MAIN	SAMSUNG ELECTRONICS PART NO. BA41-00806A
CHECK	SS BAIK	DEV. STEP	PR			
APPROVAL	KK BIN	REV	1.0		DDR2 - TERMINATION	
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	18 OF 54	

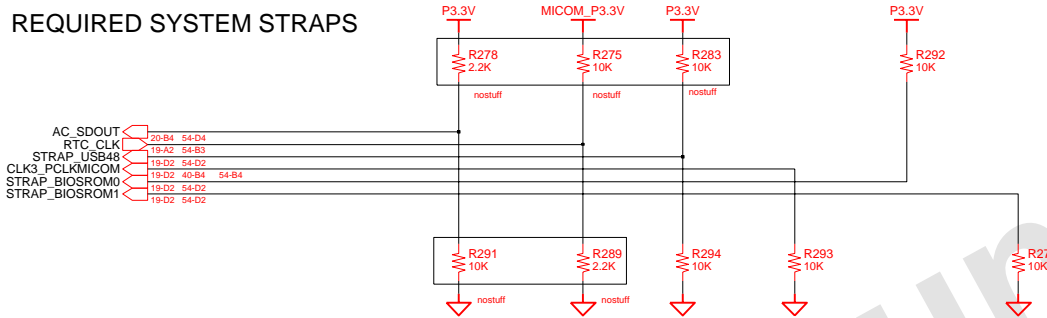






DRAM	KI IM	DATE	5/28/2007	TITLE	PRAH_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR		MAIN	
APPROVAL	KK BIN	REV	1.0		SB600(4/4)	
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	22 OF 54	

REQUIRED SYSTEM STRAPS



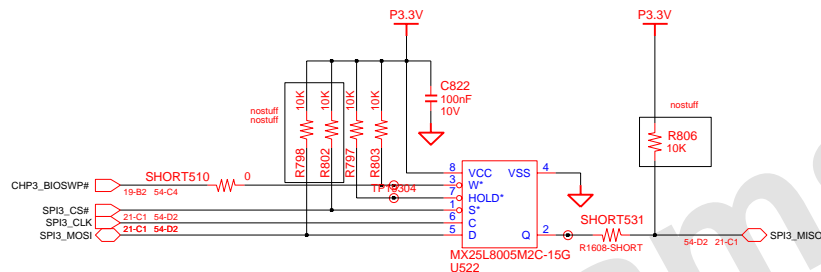
	AC_SDOUT	RTC_CLK	PCI3_CLK4	PCI3_CLK6	PCI3_CLK0	PCI3_CLK1
STRAP HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INTERNAL PLL48	CPU I/F = K8	ROM TYPE H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	
STRAP LOW	IGNORE DEBUG STRAPS	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	USE EXTERNAL 48MHz	CPU I/F = P4		

DEBUG STRAPS

	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SAMSUNG PROPRIETARY

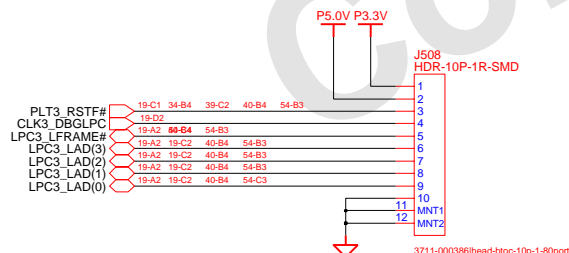
THIS DOCUMENT CONTAINS CONFIDENTIAL
PROPRIETARY INFORMATION THAT IS
SAMSUNG ELECTRONICS CO.'S PROPERTY.
DO NOT DISCLOSE TO OR DUPLICATE FOR OTHERS
EXCEPT AS AUTHORIZED BY SAMSUNG.



SPI3_CS#

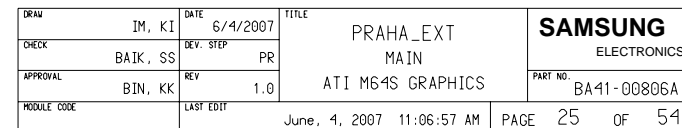
SB600 prior to A21 : Pulled up to P3.3V_ALW with 1Kohm resistor.
SB600 A21 and newer : No external pull-up resistor required.

DEBUG CARD CONN

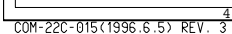


- | | | | |
|----|------------------------------------|----|---------------------------------|
| 02 | VERIFY REAL MODE | 66 | CONFIGURE ADVANCE CACHE REG. |
| 03 | DISABLE NMI | 6A | DISPLAY EXTERNAL CACHE SIZE |
| 04 | GET CPU TYPE | 6C | DISPLAY SHADOW MESSAGE |
| 06 | INIT. SYSTEM H/W | 6E | DISPLAY NON-DISPOSABLE SEGMENT |
| 08 | INIT. CHIPSET REG. | 70 | DISPLAY ERROR MESSAGE |
| 09 | SET IN POST FLAG | 72 | CHECK FOR CONFIGURATION ERROR |
| 0A | INIT CPU.REG | 74 | TEST REAL-TIME CLOCK |
| 0B | CPU CACHE ON | 76 | CHECK FOR KEYBOARD ERROR |
| 0C | INIT.CACHE TO POST | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| OE | INIT. I/O VALUE | 7E | TEST COPROCESSER IF PRESENT |
| 0F | ENABLE THE L-BUS IDE | 80 | DISABLE ON-BOARD I/O PORT |
| 10 | INIT. POWER MANAGER | 82 | DETECT AND INSTALL EXT.RS232C |
| 11 | LOAD ALTERNATE REG. | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET | 86 | RE-INIT. ON-BOARD I/O PORT |
| | WITH INITIAL POST VALUE | 88 | INIT. BIOS DATA ROM |
| 14 | INIT. KEYBOARD CONTROLLER | 8A | INIT.EXTENDED BIOS DATA AREA |
| 16 | CHECK CHECKSUM | 8C | INIT. FDD CONTROLLER |
| 18 | 8254 TIMER INIT. | 9A | SHADOW OPTION ROMS |
| 1A | 8237 DMA CONTROLLER INIT. | 9C | SETUP POWER MANAGEMENT |
| 1C | RESET INTERRUPT CONTROLLER | 9E | ENABLE H/W INTERRUPT |
| 20 | TEST DRAM REFRESH | A0 | SET TIME OF DAY |
| 22 | TEST 8742 KEYBOARD CONTROLLER | A4 | INIT. TYPEMATIC RATE |
| 24 | SET ES SEGMENT REG. TO 4GB | A8 | ERASE F2 PROMPT |
| 26 | ENABLE A20 | AA | SCAN FOR F2 KEY STROKE |
| 28 | AUTO SIZING DRAM | AC | ENTER SETUP |
| 32 | COMPUTE THE CPU SPEED | AE | CLEAR IN POST FLAG |
| 34 | TEST CMOS RAM | B0 | CHECK FOR ERRORS |
| 38 | SHADOW SYSTEM BIOS ROM | B2 | POST DONE-PREPARE TO BOOT O/S |
| 3A | AUTO SIZING CACHE | B4 | ONE BEEP |
| 3C | CONFIGURE ADVANCED CHIPSET REG. | B6 | CHECK PASSWORD (OPTION) |
| 3D | LOAD ALTER REG. WITH CMOS VALUE | B7 | ACPI INIT |
| 42 | INIT. INTERRUPT VECTOR | BA | DMI INIT |
| 44 | INIT. BIOS INTERRUPT | BE | CLEAR SCREEN |
| 46 | CHECK ROM COPYRIGHT NOTICE | C0 | TRY BOOT WITH INT19 |
| 47 | INIT. I20 SUPPORT IF INSTALLED | D0 | INTERRUPT HANDLER ERROR |
| 48 | CHECK VIDEO CONFIGURE AGAINST CMOS | D2 | UNKNOWN INTERRUPT ERROR |
| 49 | INIT. PCI BUS AND DEVICE | D4 | PENDING INTERRUPT ERROR |
| 4A | INIT. ALL VIDEO BIOS ROM | D6 | SHUTDOWN 5 |
| 4C | SHADOW VIDEO BIOS ROM | D8 | SHUTDOWN ERROR |
| 50 | DISPLAY CPU TYPE AND SPEED | DA | EXTENDED BLOCK MOVE |
| 52 | TEST KEYBOARD | DC | SHUTDOWN 10 |
| 54 | SET KEYCLICK IF ENABLED | 89 | ENABLE NMI |
| 56 | ENABLE KEYBOARD | 90 | INIT. HDD CONTROLLER |
| 58 | TEST FOR UNEXPECTED INTERRUPTS | 91 | INIT. LOCAL BUS HDD CONTROLLER |
| 5A | DISPLAY "PRESS SETUP" | 92 | JUMP TO USER PATCH 2 |
| 5C | TEST RAM BETWEEN 512K AND 640K | 94 | DISABLE A20 ADDRESS LINE |
| 60 | TEST EXTENDED MEMORY | 96 | CLEAR HUGE ES SEGMENT REG. |
| 62 | TEST EXTENDED MEMORY ADDRESS LINE | 98 | SEARCH FOR OPTION ROMS |
| 64 | JUMP TO USER PATCH 1 | | |

DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG
CHECK	SS BAIK	DEV. STEP	PR		MAIN	ELECTRONICS
APPROVAL	KK BIN	REV	1.0	SPI ROM & DEBUG PORT	PART NO.	BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	24	OF 54

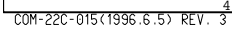


THIS DOCUMENT CONTAINS CONFIDENTIAL
PROPRIETARY INFORMATION THAT IS
SAMSUNG ELECTRONICS CO'S PROPERTY.
NOT DISCLOSE TO OR DUPLICATE FOR OTHERS
EXCEPT AS AUTHORIZED BY SAMSUNG.

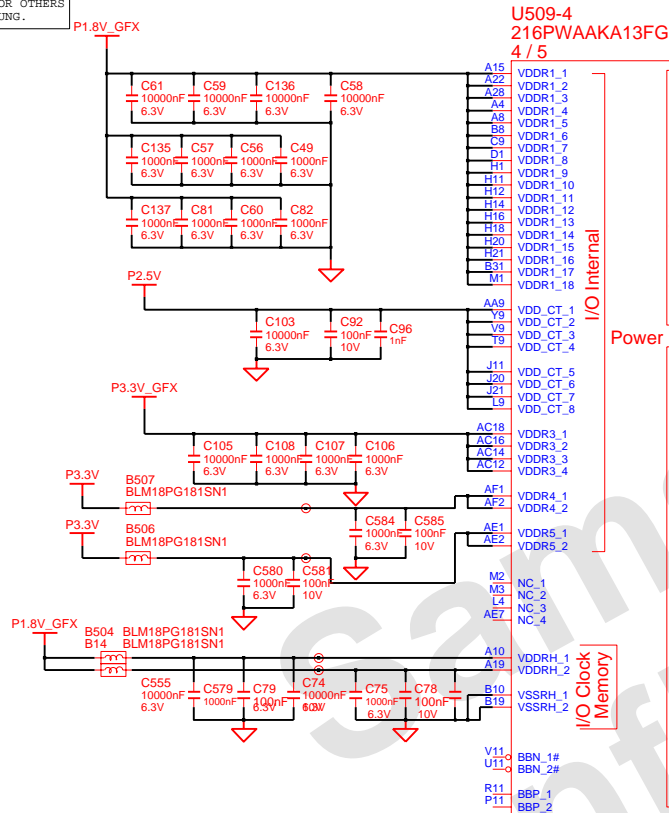


d:/users/mobile20/mentor/praha/pr_order/praha_main_

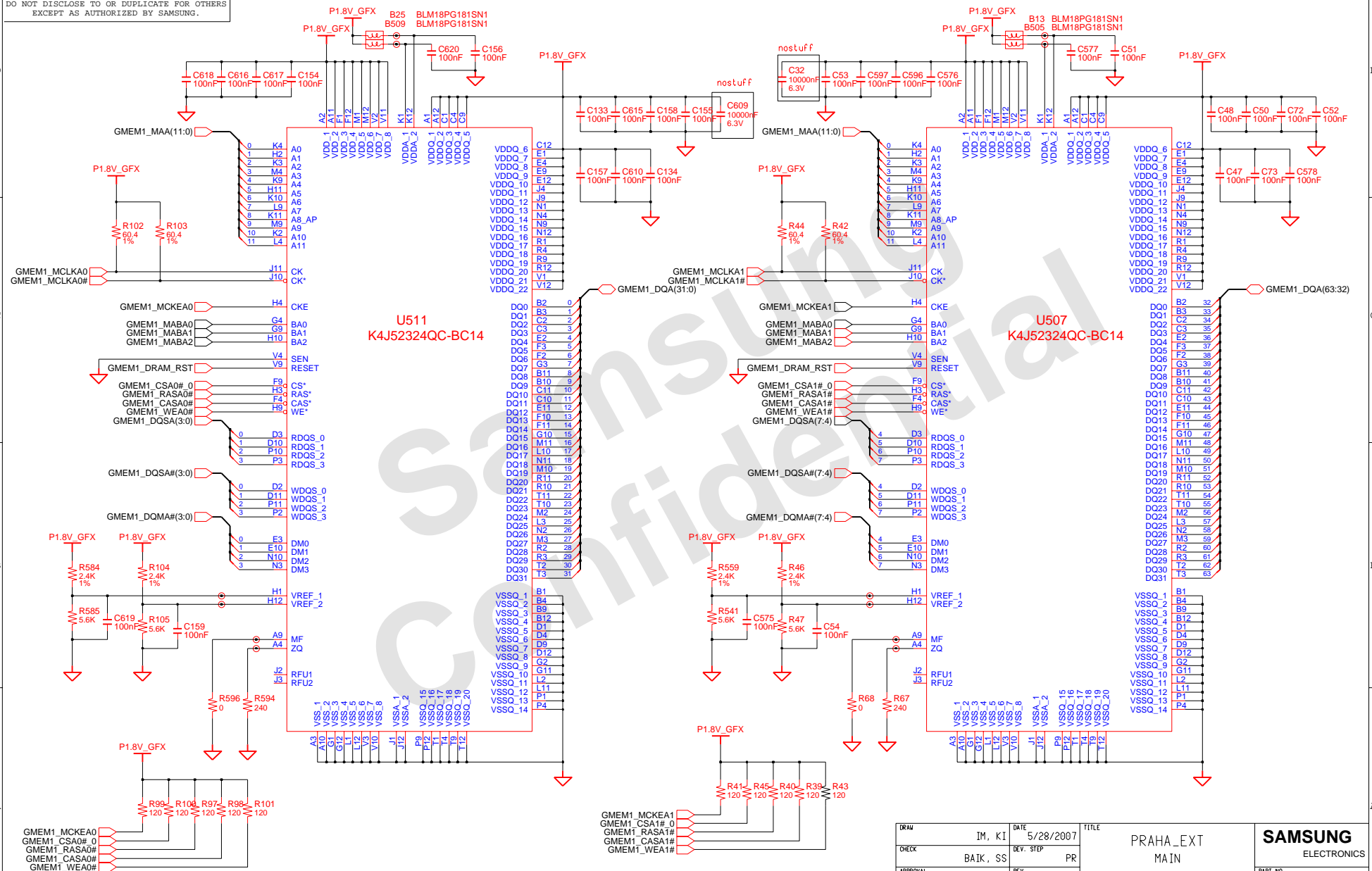
THIS DOCUMENT CONTAINS CONFIDENTIAL
PROPRIETARY INFORMATION THAT IS
SAMSUNG ELECTRONICS CO'S PROPERTY.
NOT DISCLOSE TO OR DUPLICATE FOR OTHERS
EXCEPT AS AUTHORIZED BY SAMSUNG.



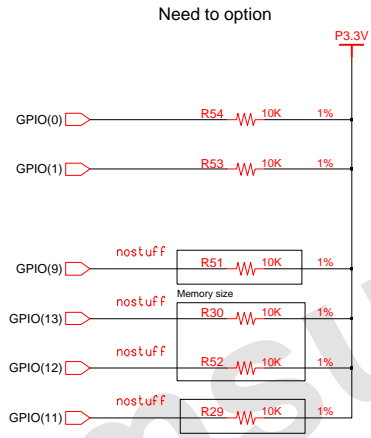
d:/users/mobile20/mentor/praha/pr_order/praha_main_



A-channel



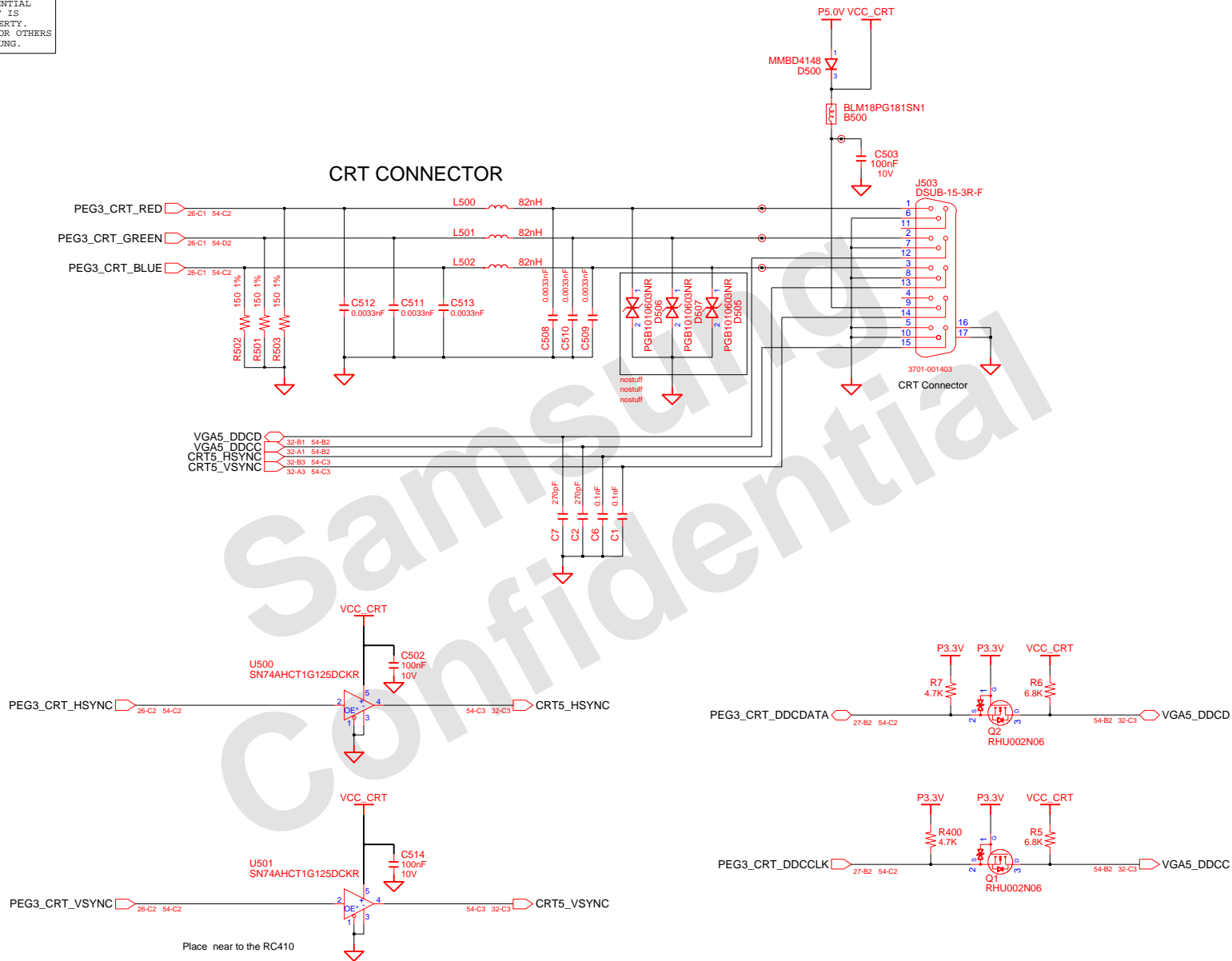
DRAW		IM, KI	DATE	5/28/2007	TITLE		PRAHA_EXT		SAMSUNG ELECTRONICS	
CHECK		BAIK, SS	DES. STEP	PR			MAIN			
APPROVAL		BIN, KK	REV	1.0			ATI M64S GRAPHICS		PART NO.	
MODULE CODE		LAST EDIT		June, 4, 2007 11:09:15 AM				PAGE	29	OF 54



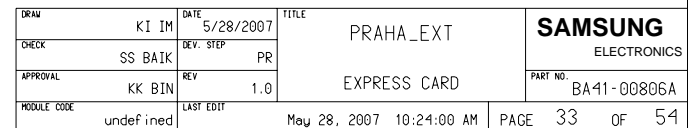
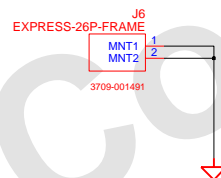
(DEFAULT : pull-down)

STRAP	PIN	DESCRIPTION
TX_PWRS_ENB	GPIO[0]	Transmitter Power Saving Enable 0: 50% Tx output swing 1: full Tx output swing
TX_DEEMPH_EN	GPIO[1]	Transmitter De-emphasis Enable 0: Tx De-emphasis disabled 1: Tx de-emphasis enabled
DEBUG_ACCESS	GPIO[4]	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.
ROMIDCFG[3:0]	GPIO[9,13:11]	When no ROM is attached, GPIO[9] is set to 0. GPIO[13:12] is used to select the frame buffer aperture size. GPIO[13:12] = 00: 128M frame buffer GPIO[13:12] = 01: 256M frame buffer GPIO[13:12] = 10: 64M frame buffer GPIO[13:12] = 11: reserved

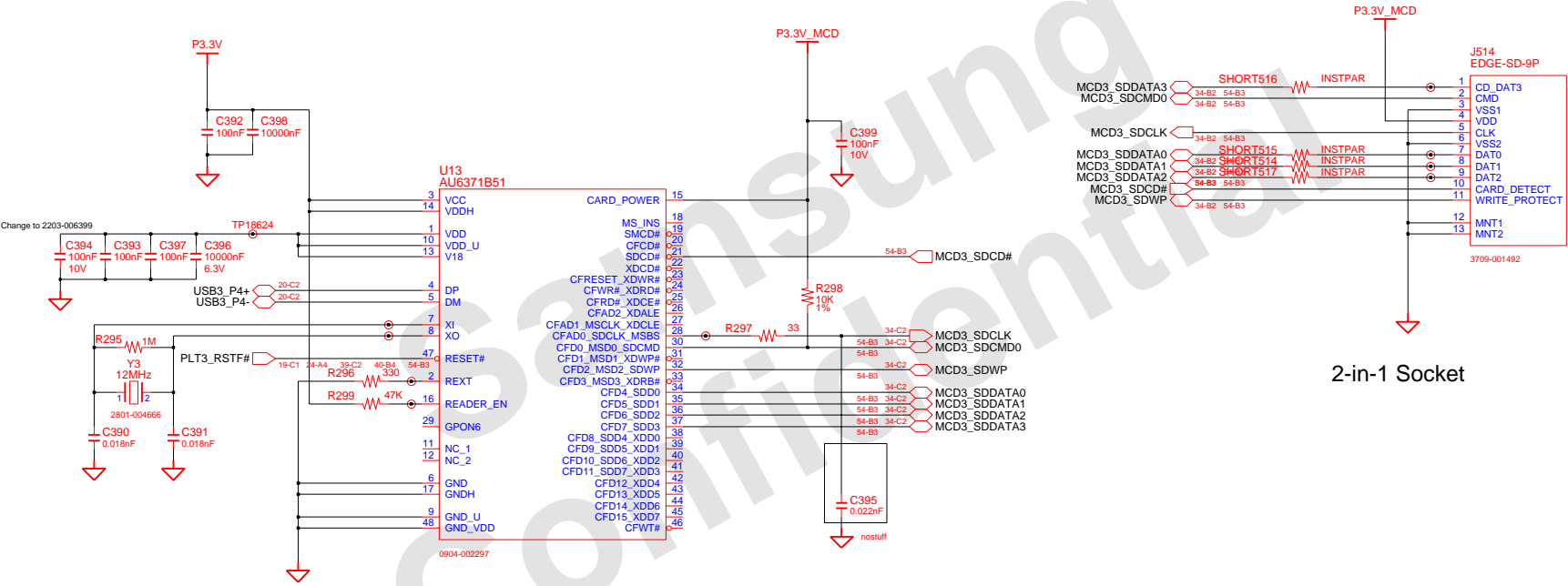
THIS DOCUMENT CONTAINS CONFIDENTIAL
PROPRIETARY INFORMATION THAT IS
SAMSUNG ELECTRONICS CO'S PROPERTY.
DO NOT DISCLOSE TO OR DUPLICATE FOR OTHERS
EXCEPT AS AUTHORIZED BY SAMSUNG.



DRAW		DATE	TITLE		SAMSUNG ELECTRONICS	
KI IM		5/28/2007	PRAHA_EXT			
CHECK	SS BAIK	REV. STEP	CRT		PART NO.	
APPROVAL	KK BIN	REV	1.0		BA41-00806A	
MODULE CODE		LAST EDIT		PAGE		
undefined		May 28, 2007 10:24:00 AM		32		OF 54

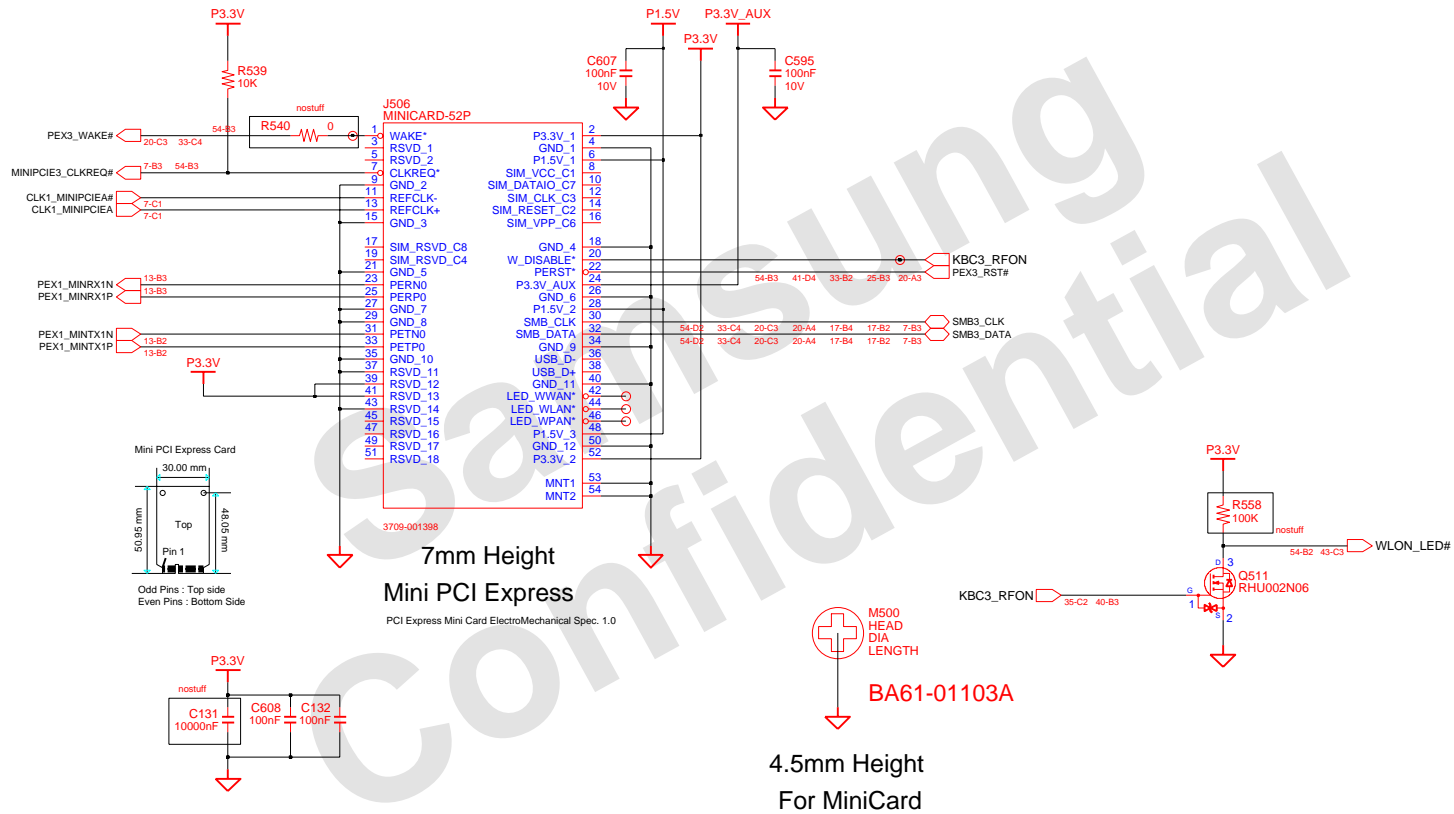


2 IN 1 CARD

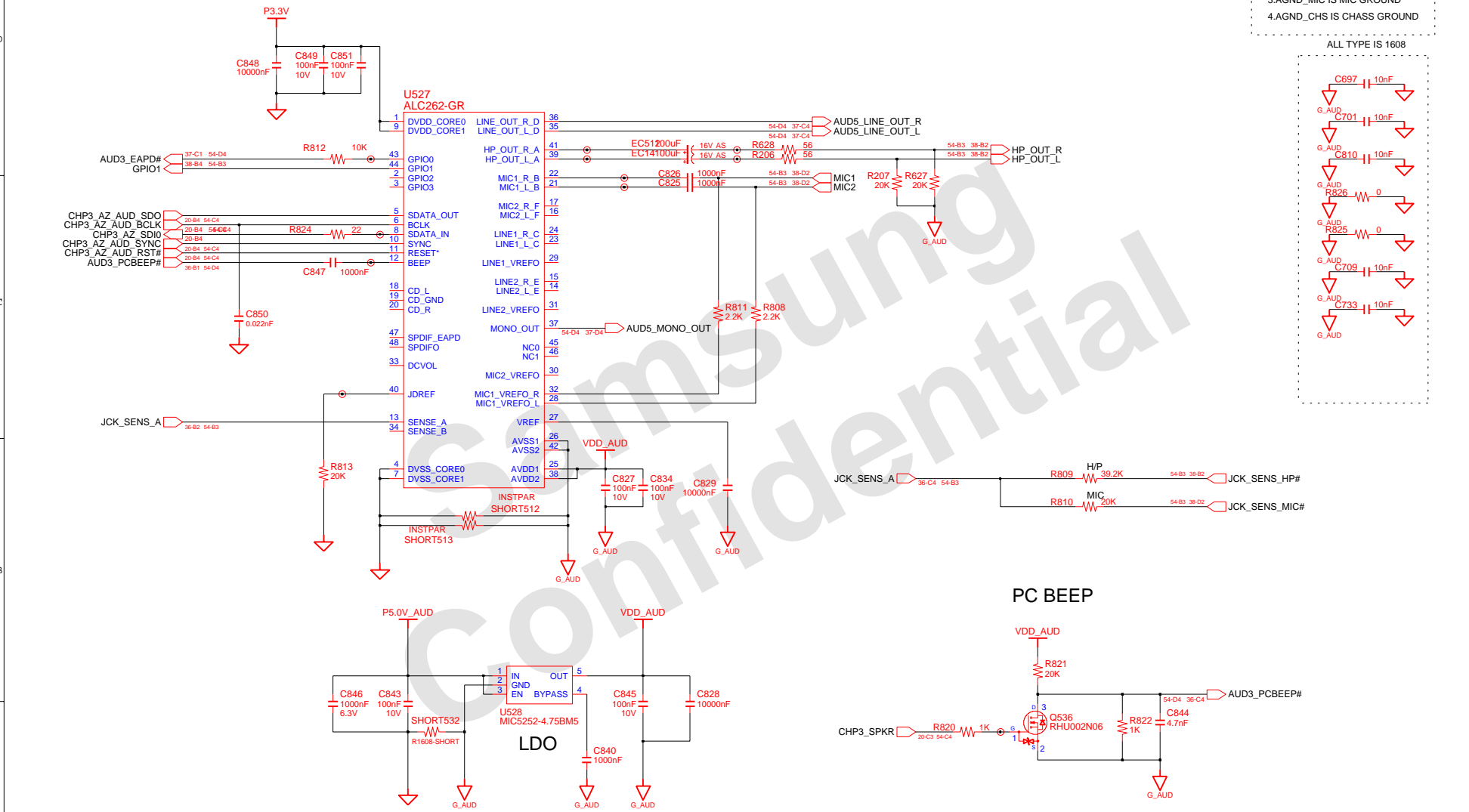


2-in-1 Socket

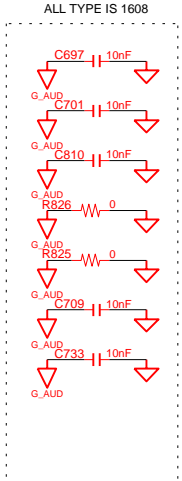
DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00806A
CHECK	SS BAIK	DEV. STEP	PR			
APPROVAL	KK BIN	REV	1.0	2 in 1 Socket		
MODULE CODE		LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	34 OF 54	



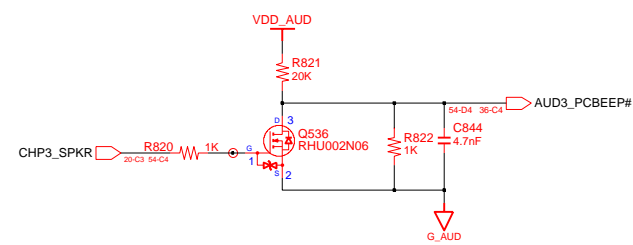
DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR		MAIN	
APPROVAL	KK BIN	REV	1.0		MINI CARD	PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	35	OF 54



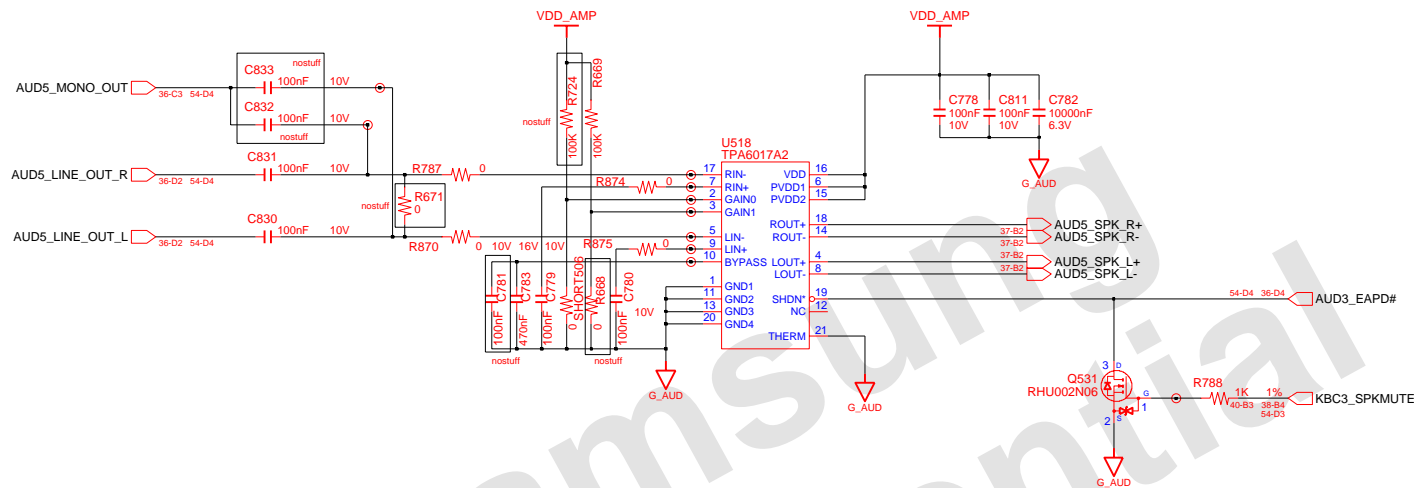
- 1.AGND_AUD IS AUDIO GROUND
- 2. GND IS DIGITAL GROUND
- 3.AGND_MIC IS MIC GROUND
- 4.AGND_CHS IS CHASSIS GROUND



PC BEEP

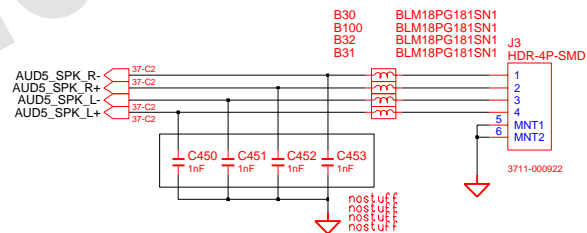
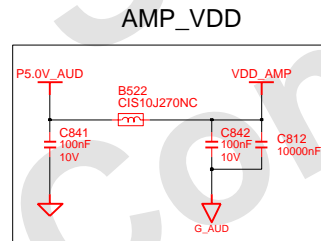


DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT MAIN AUDIO CODEC	SAMSUNG ELECTRONICS PART NO. BA41-00806A
CHECK	SS BAIK	DEV. STEP	PR			
APPROVAL	KK BIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	36 OF 54	



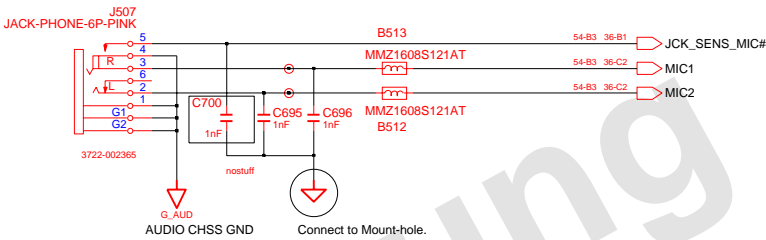
INTERNAL STEREO SPEAKERS

The trace bigger than 30mil

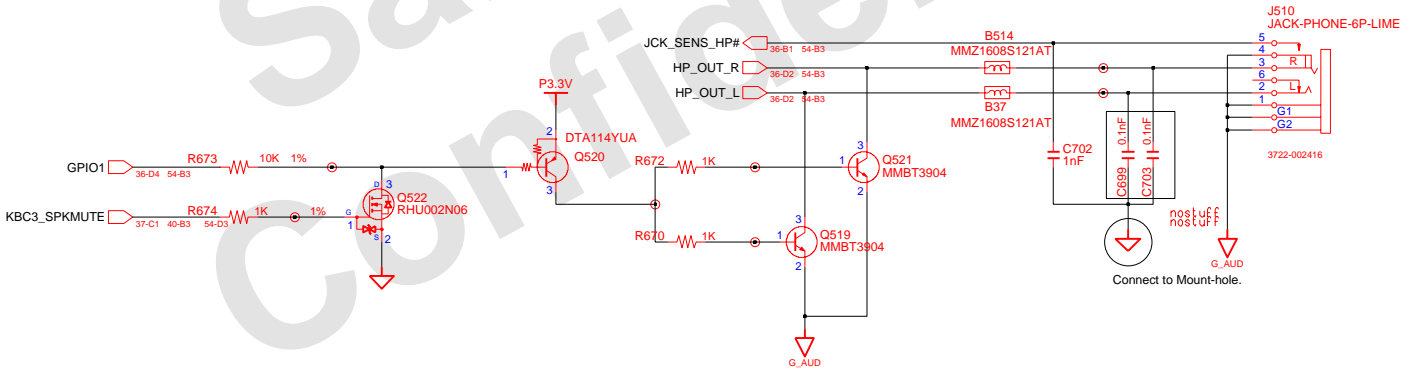


DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT MAIN LIMITER & AMP	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	REV	1.0	PART NO. BA41-00806A
APPROVAL	KK BIN	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	37	OF 54
MODULE CODE	undefined					

MIC JACK

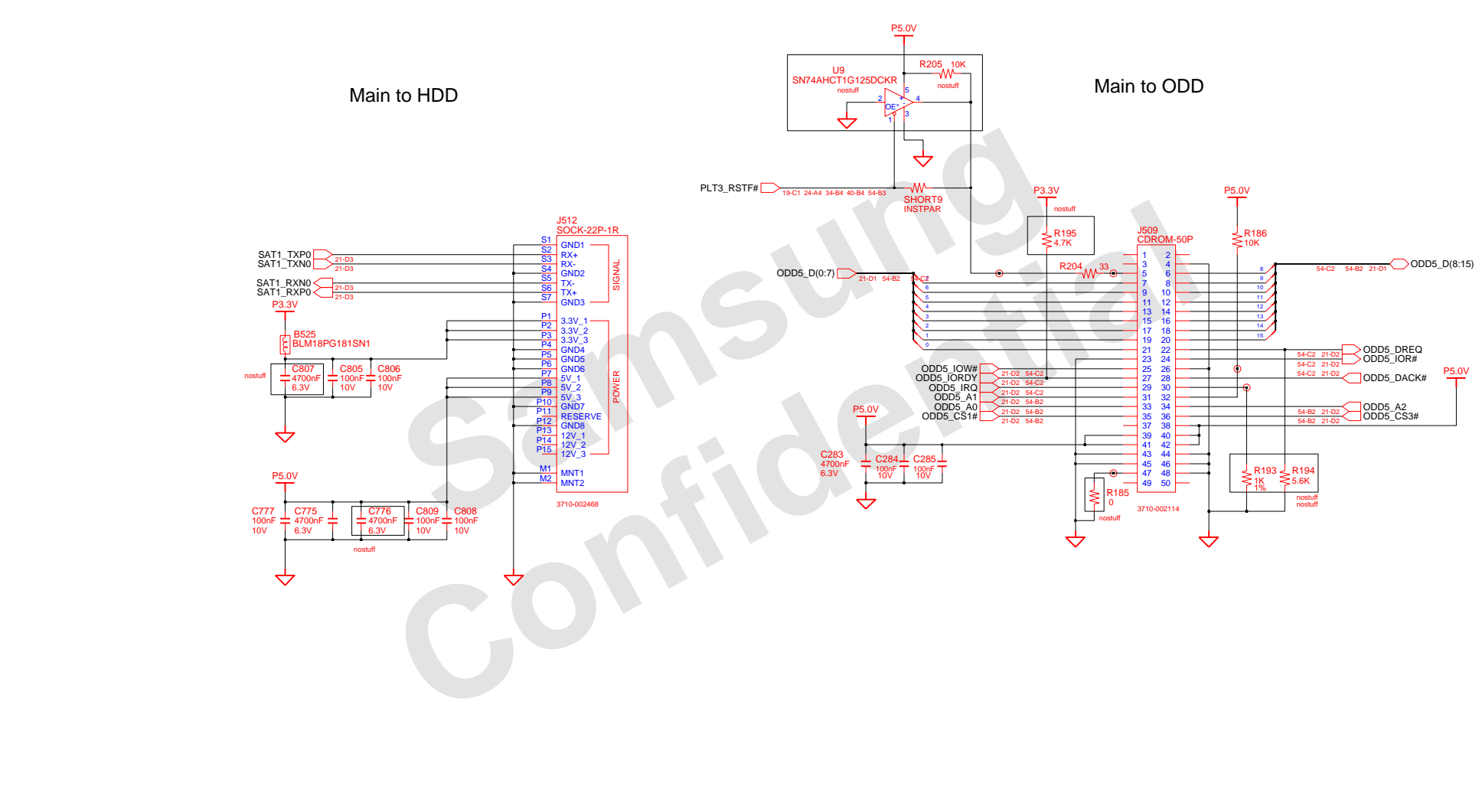


HEADPHONE



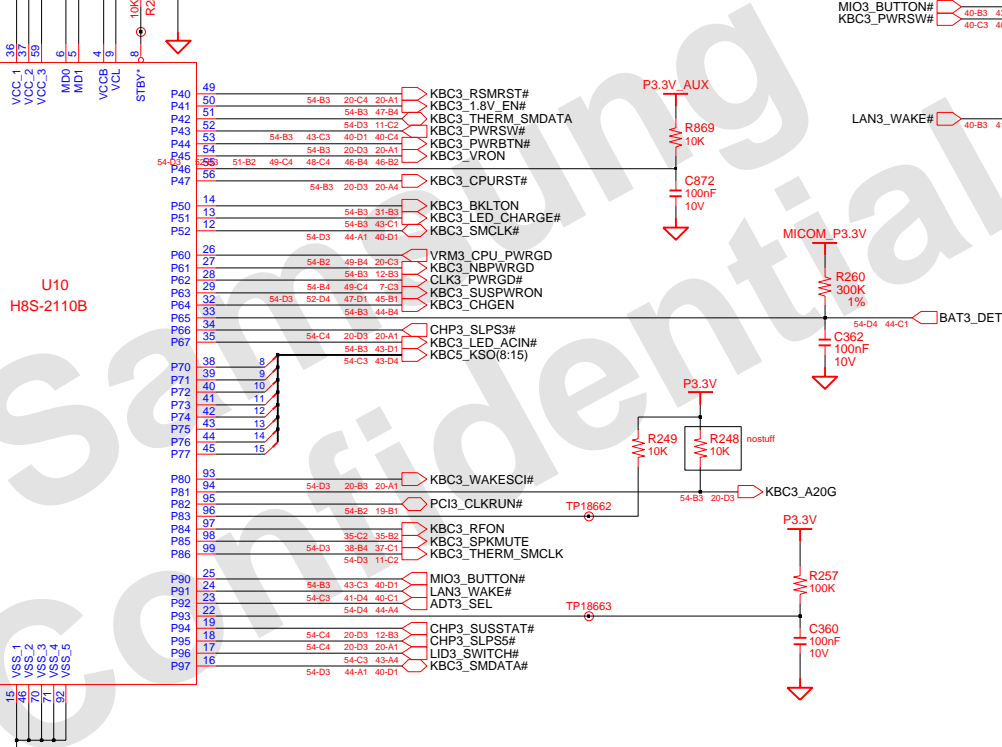
The traces led to Audio Jacks have the width over 10mil

DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT MAIN MIC & HEADPHONE	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	REV	1.0	PART NO. BA41-00806A
APPROVAL	KK BIN	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	38	OF 54
MODULE CODE	undefined					



DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT POWER HDD & ODD	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR			PART NO. BA41-00806A
APPROVAL	KK BIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	39	OF 54

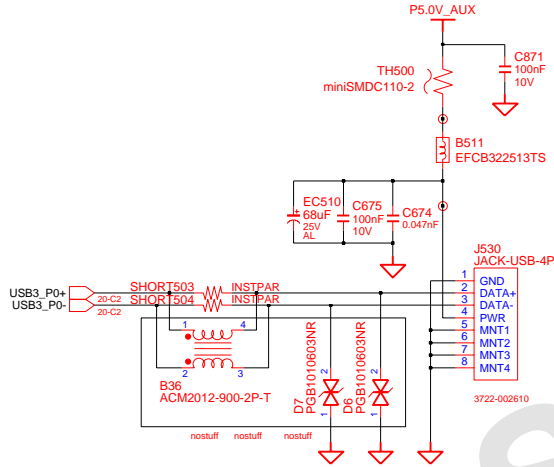
THIS DOCUMENT CONTAINS CONFIDENTIAL
PROPRIETARY INFORMATION THAT IS
SAMSUNG ELECTRONICS CO'S PROPERTY.
NOT DISCLOSE TO OR DUPLICATE FOR OTHERS
EXCEPT AS AUTHORIZED BY SAMSUNG.



PART NO. BA41-00806

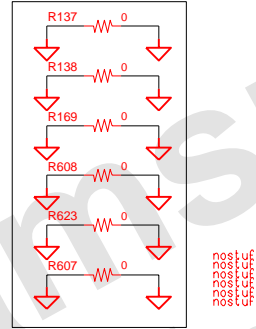
Check if need USB Power S/W(TPS2062)

Side USB Connector



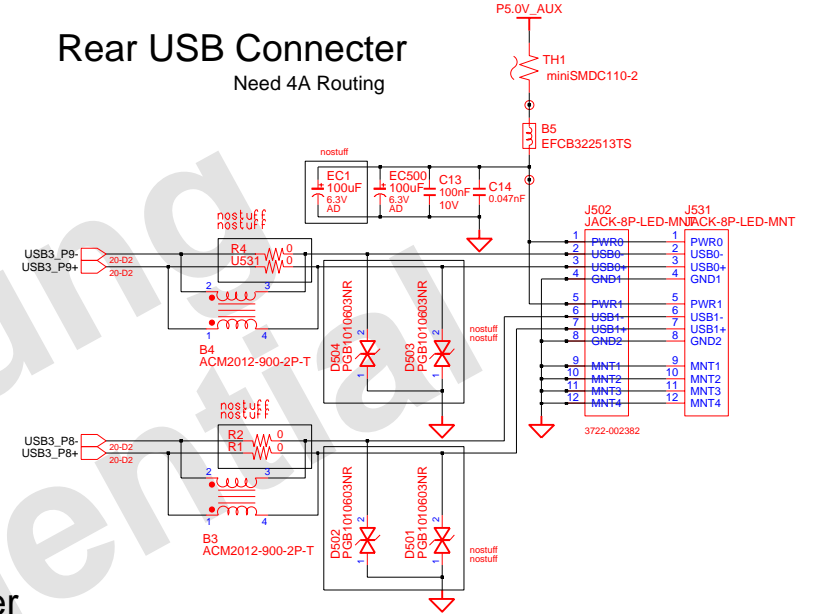
Connect left side USB GND with CPU GND

Top : 3EA Bottom : 3EA

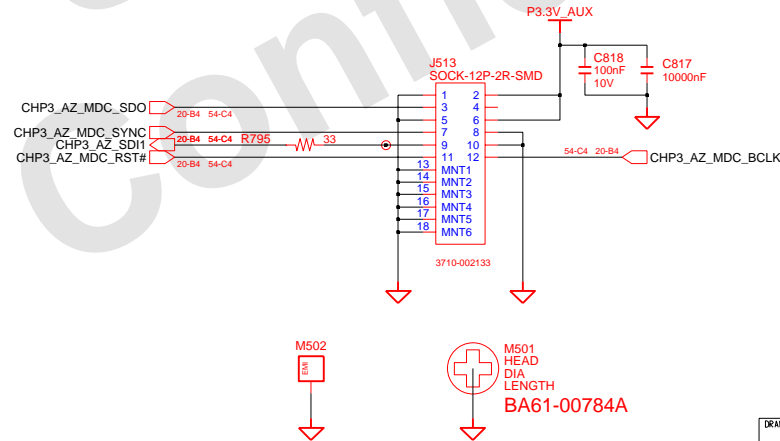


Rear USB Connector

Need 4A Routing

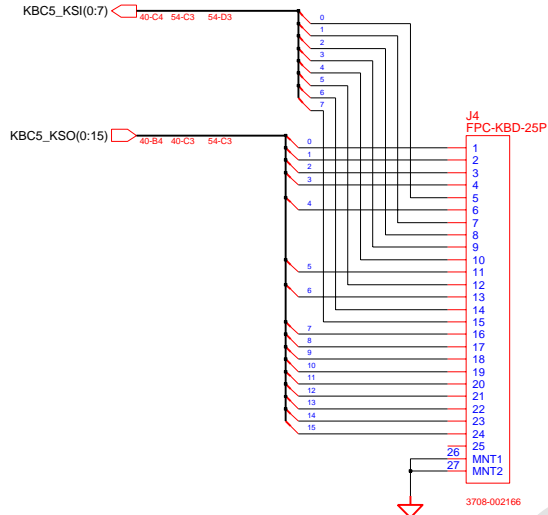


MDC Connector

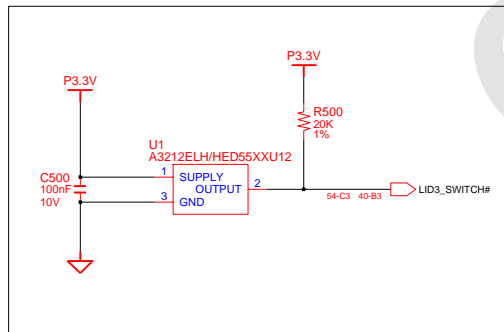


DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG
CHECK	SS BAIK	DEV. STEP	PR		MAIN	ELECTRONICS
APPROVAL	KK BIN	REV	1.0	USB PORT & MDC Conn.		PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	42	OF 54

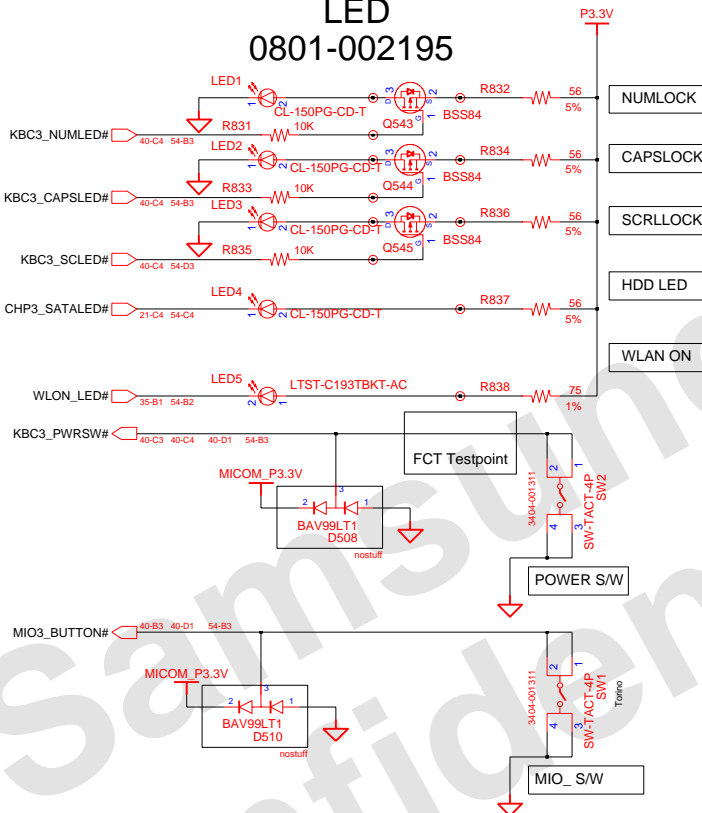
KEYBOARD



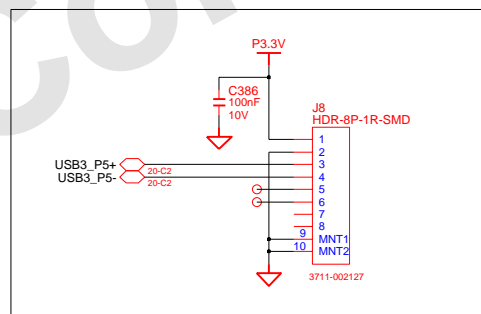
LID SWITCH



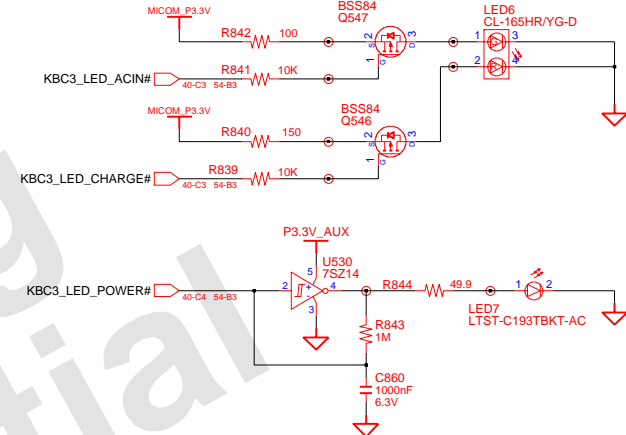
LED 0801-002195



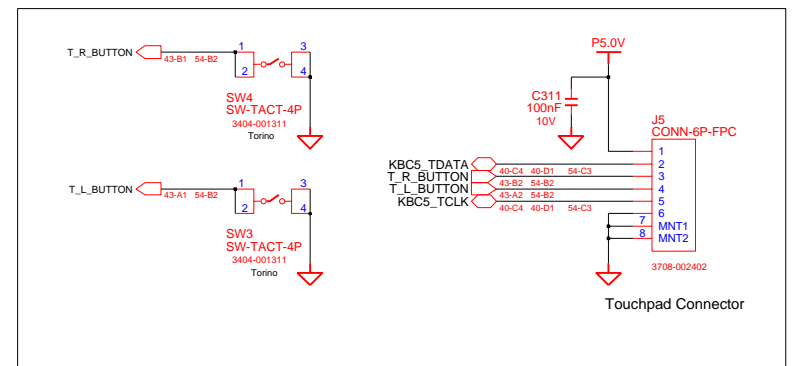
Bluetooth Interface Factory Option



ADAPTERIN/CHARGING LED



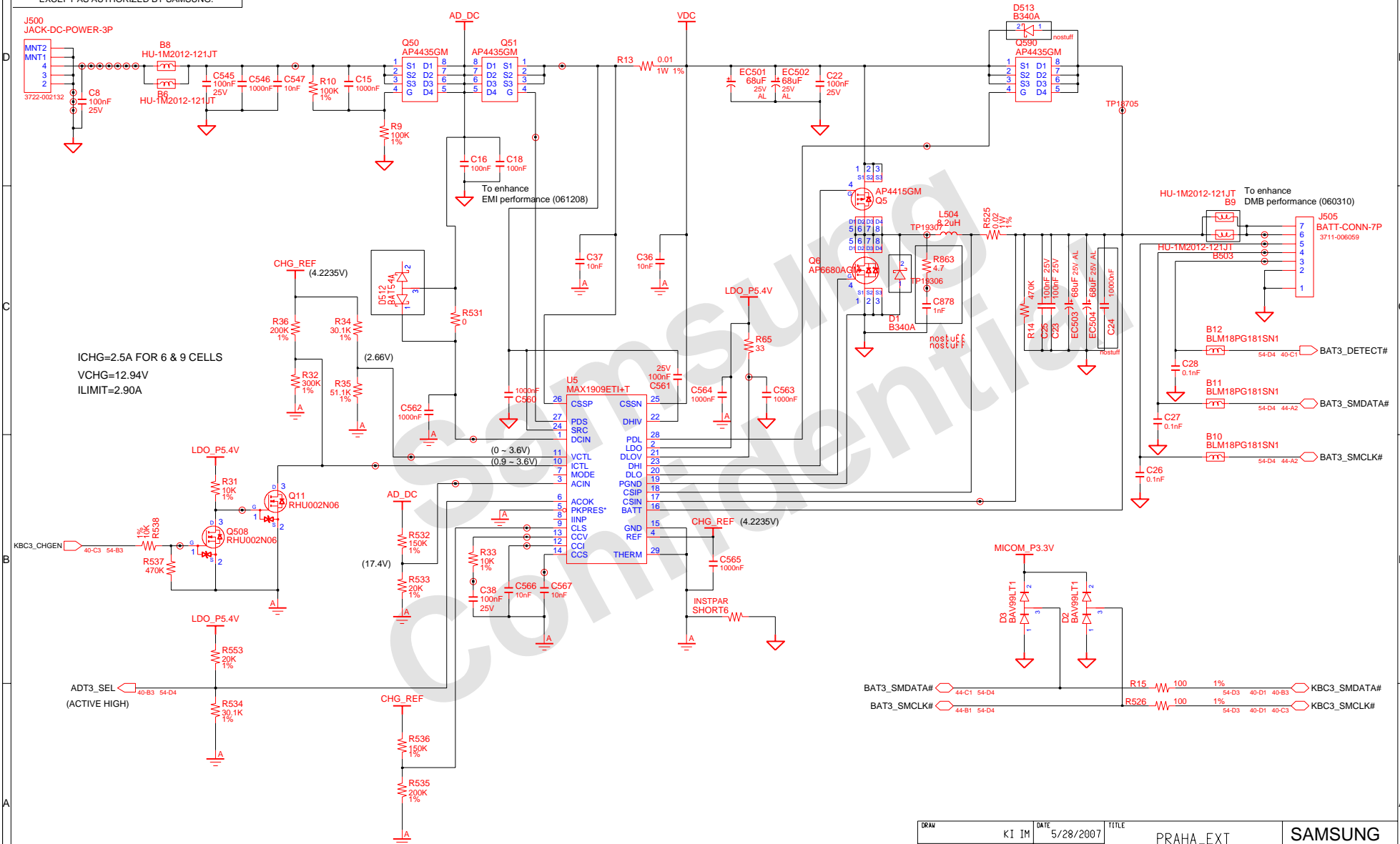
TOUCHPAD



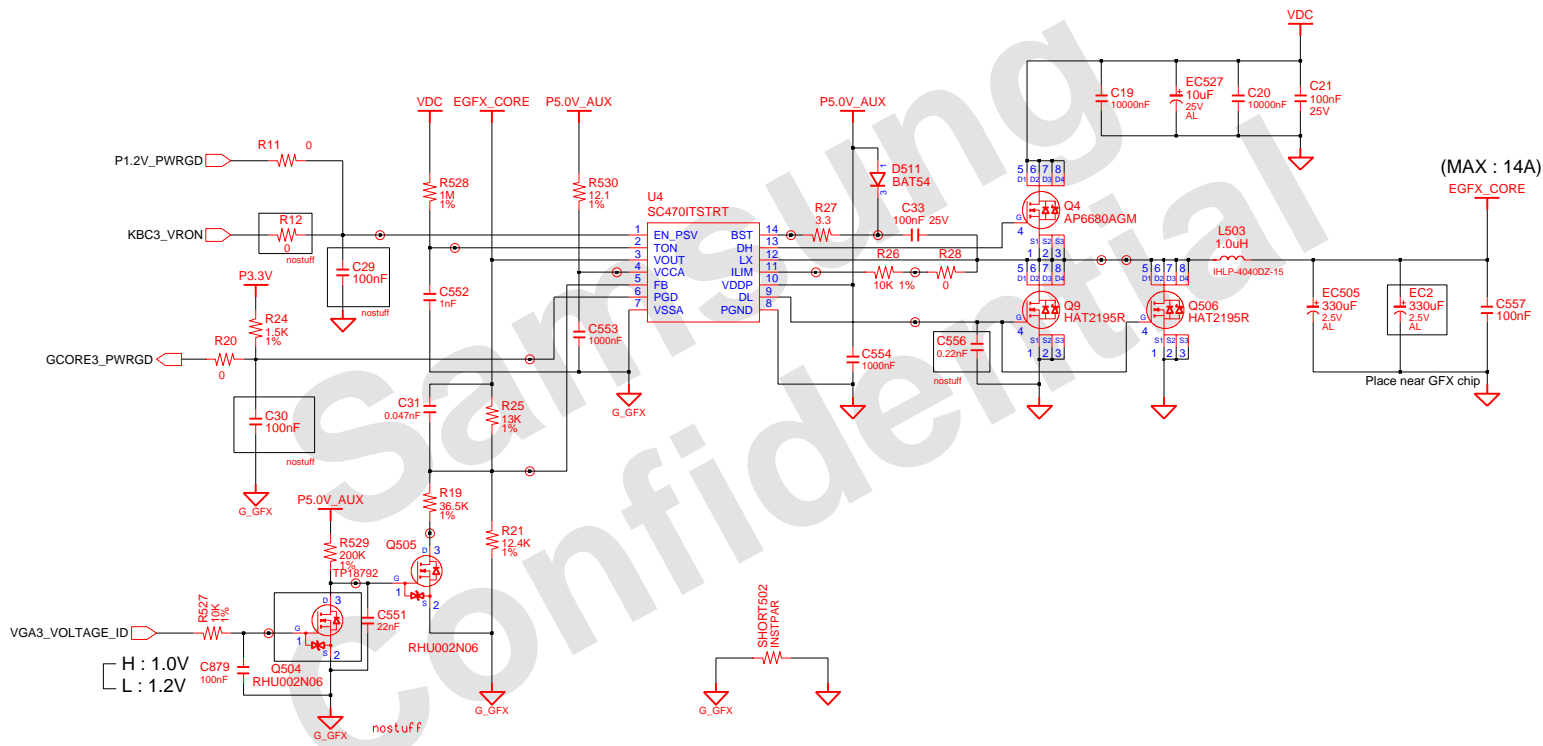
DRAW	KI IM	DATE	5/28/2007	TITLE	PRaha_EXT
CHECK	SS BAIK	DEV. STEP	PR		LED & BLUETOOTH
APPROVAL	KK BIN	REV	1.0		TOUCHPAD & KBD & LID S/W
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	43 OF 54

SAMSUNG ELECTRONICS	PART NO.	BA41-00806A
-------------------------------	----------	-------------

CHARGER & POWER MANAGEMENT

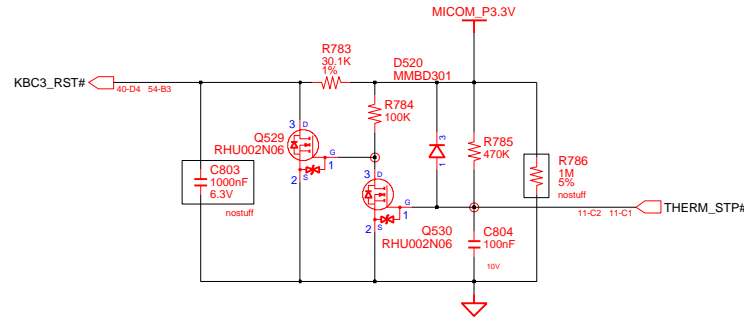


GFX CORE [SEMTECH]

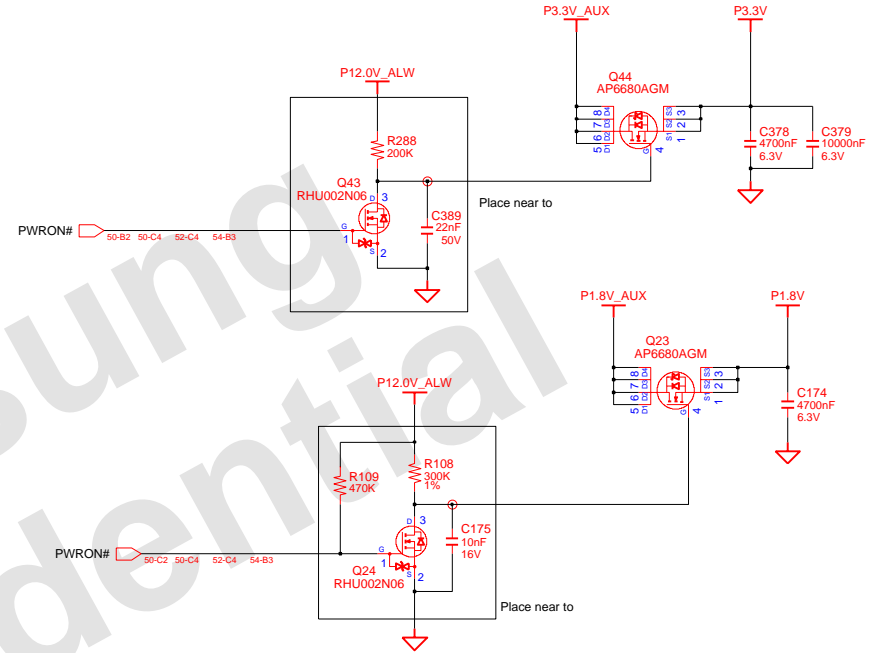


DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG
CHECK	SS BAIK	DEV. STEP	PR		UNDEFINED	ELECTRONICS
APPROVAL	KK BIN	REV	1.0		UNDEFINED	PART NO. BA41-00806A
MODULE CODE		LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	48	OF 54

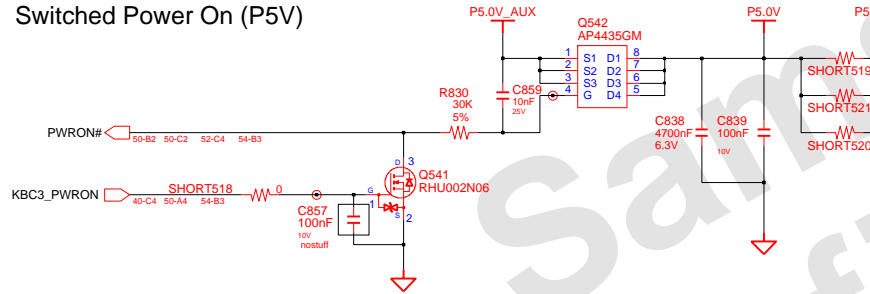
MICOM RESET



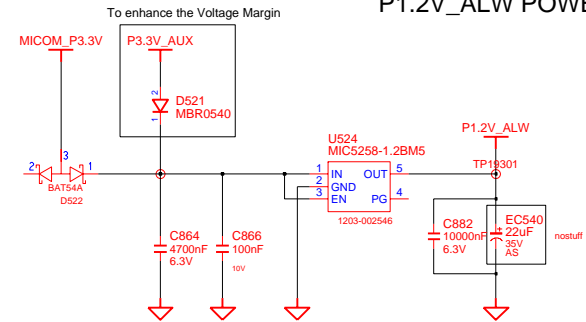
Switched Power On (P3.3V & 1.8V)



Switched Power On (P5V)

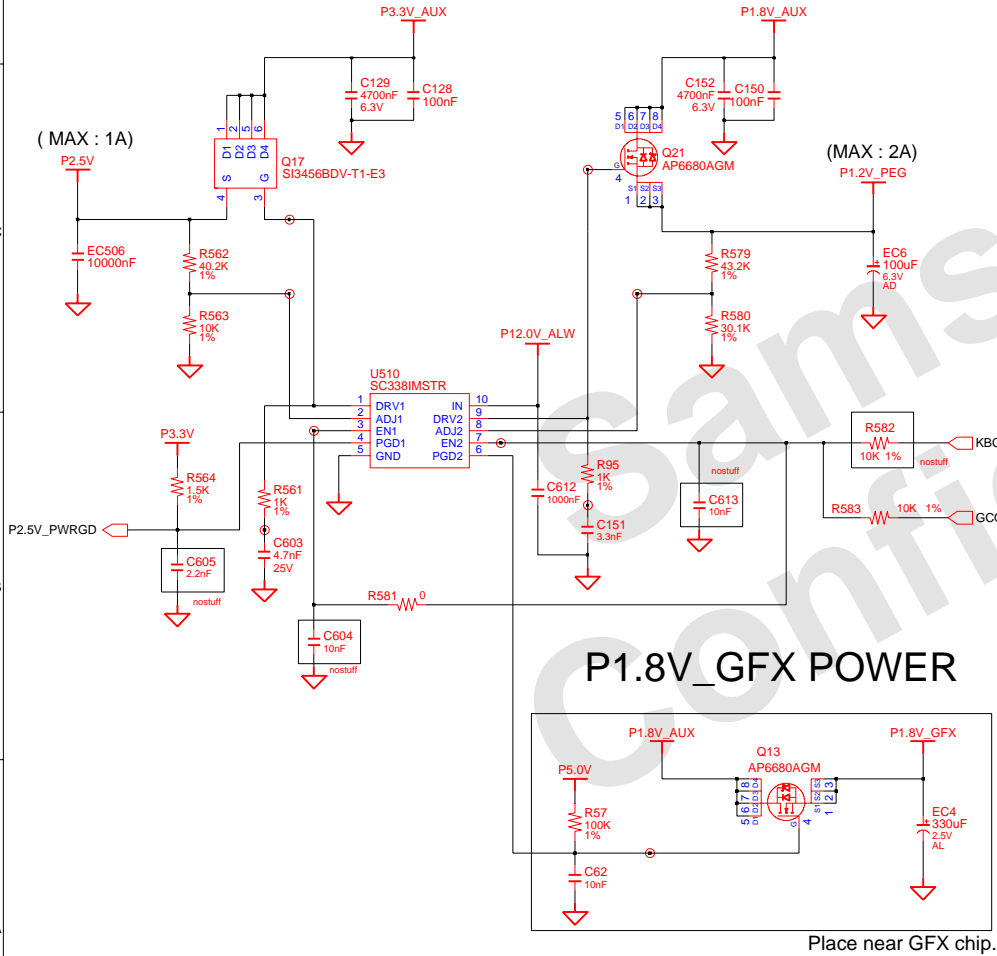


P1.2V_ALW POWER

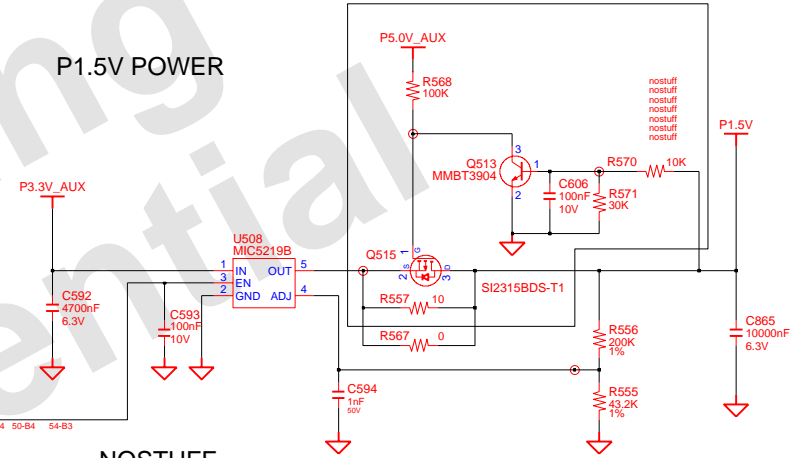


DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT MAIN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR			
APPROVAL	KK BIN	REV	1.0	MICOM & SWITCHED POWER	PART NO. BA41-00806A	
MODULE CODE	undefined	LAST EDIT		May 28, 2007 10:24:00 AM	PAGE 50 OF 54	

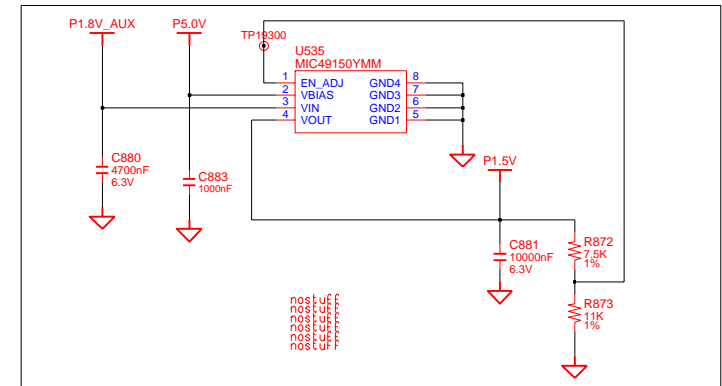
P1.2V_NB / P2.5V POWER



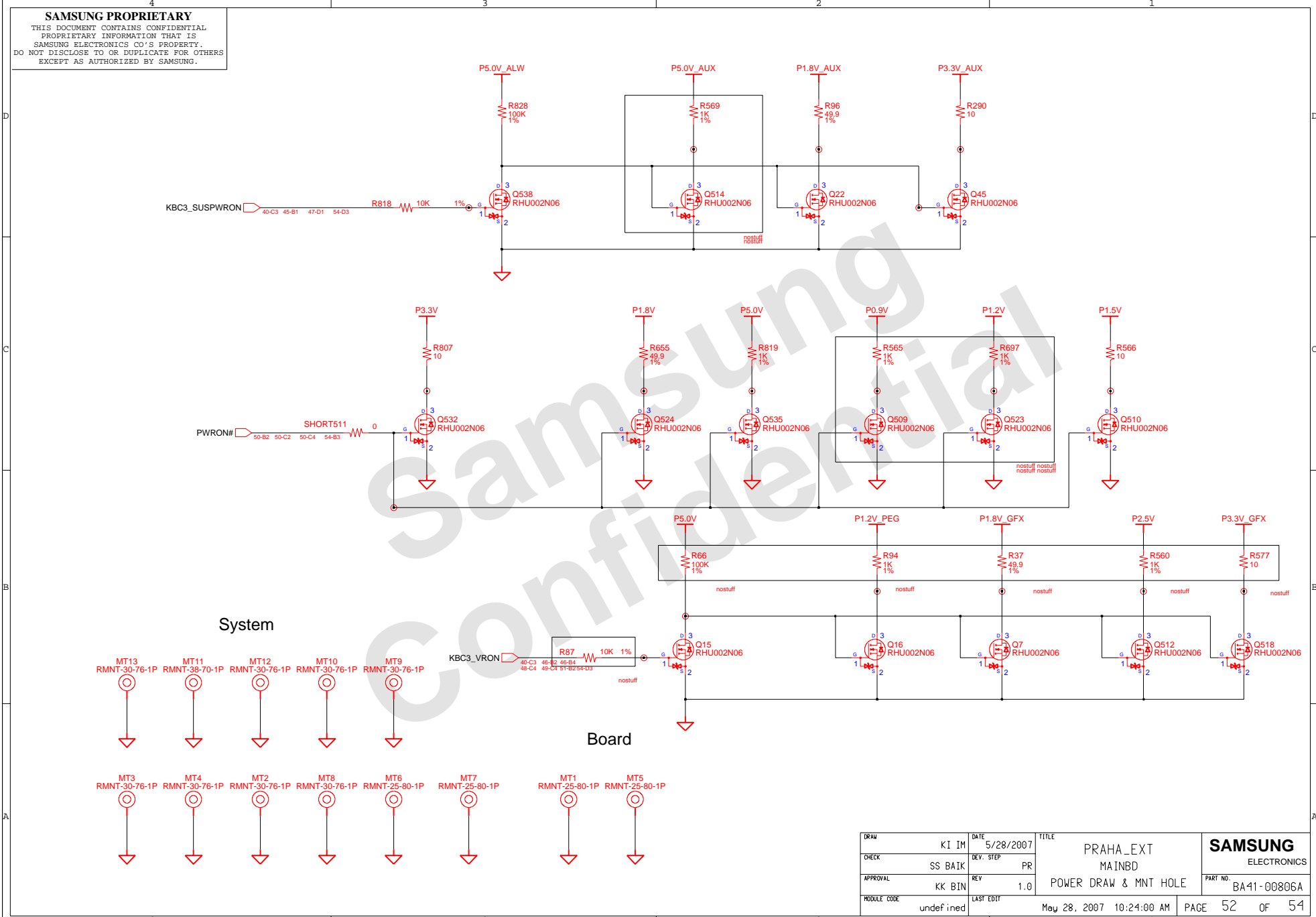
P1.5V POWER

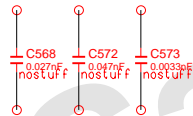
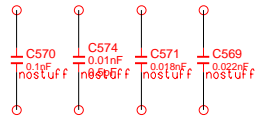
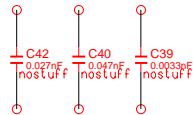
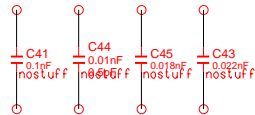


NOSTUFF



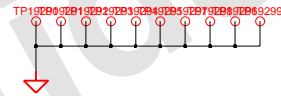
DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG
CHECK	SS BAIK	DEV. STEP	PR			ELECTRONICS
APPROVAL	KK BIN	REV	1.0		ICT PORT	PART NO.
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	51	BA411-00806A
				OF	54	



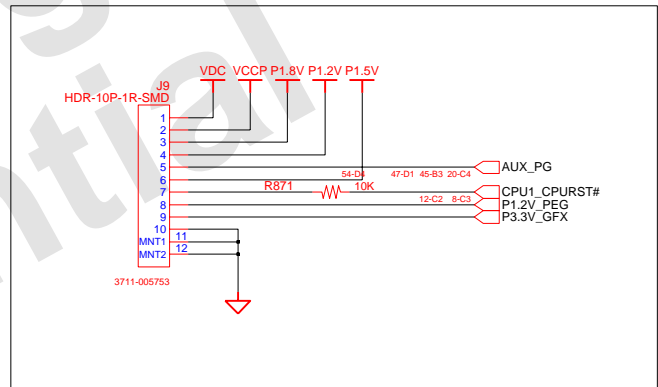


REV1
1
2 0 03

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			



ICT PORT



DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG
CHECK	SS BAIK	DEV. STEP	PR			ELECTRONICS
APPROVAL	KK BIN	REV	1.0	TP		PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	53	OF 54

THIS DOCUMENT CONTAINS CONFIDENTIAL
PROPRIETARY INFORMATION THAT IS
SAMSUNG ELECTRONICS CO'S PROPERTY.
DO NOT DISCLOSE TO OR DUPLICATE FOR OTHERS
EXCEPT AS AUTHORIZED BY SAMSUNG.

```
TP18962 CPU1_DBSY#
TP18963 CPU1_DEFERR#
TP18964 CPU1_DPRSTP#
TP18965 CPU1_DPSLP#
TP18966 CPU1_DPRW#
TP18967 CPU1_DRDY#
TP18939 CPU1_FERR#
TP18940 CPU1_HIT#
TP18941 CPU1_HITM#
TP18942 CPU1_IGNNE#
TP18943 CPU1_INIT#
TP18944 CPU1_INTR#
TP18945 CPU1_LOCK#
TP18946 CPU1_NMI#
TP18947 CPU1_PSI#
TP18948 CPU1_PURGPCPU1
```

```
TP18905#HP_OUT_R#
TP18906#TP3_DBRESET#
TP18907#TP3_SYSTRST#
TP18908#QCK_SENS_A#
TP18909#QCK_SENS_HP#
TP18910#QCK_SENS_MIC#
TP18911#KB3C3_1_8V_EN#
TP18912#KB3C3_1_8V_EN#
TP18913#KB3C3_BKL_TN#
TP18865#KB3C3_CAPLED#
TP18866#KB3C3_CHGEN#
TP18867#KB3C3_CPURST#
TP18868#KB3C3_EXTSMI#
TP18869#KB3C3_LED_ACIN#
TP18870#KB3C3_LED_CHARG#
TP18871#KB3C3_LED_POWER#
TP18872#KB3C3_NBPWRM#
TP18873#KB3C3_NUMLED#
TP18874#KB3C3_PWRBTN#
TP18875#KB3C3_PWRGD#
TP18876#KB3C3_PWRON#
TP18877#KB3C3_PWSW#
TP18878#KB3C3_RST#
TP18879#KB3C3_RST#
TP18880#KB3C3_RSTNC#
```

T18881(KBC3_SCLC#)
T18882(KBC3_SMDL#)
T18883(KBC3_SMDATA#)
T18884(KBC3_SMUPA#)
T18885(KBC3_SMUPA#)
T18886(KBC3_THERM_SMLC)
T18887(KBC3_THERM_SMDATA)
T18888(KBC3_VRO#)
T18889(KBC5_CSC#)
T18890(KBC5_KS1#)
T18891(KBC5_KS1(1))
T18892(KBC5_KS1(2))
T18893(KBC5_KS1(3))
T18894(KBC5_KS1(4))
T18895(KBC5_KS1(5))
T18896(KBC5_KS1(6))
T18897(KBC5_KS1(7))
T18898(KBC5_KS1(8))
T18899(KBC5_KS1(9))
T18900(KBC5_KS1(10))
T18901(KBC5_KS1(11))
T18902(KBC5_KS1(12))
T18903(KBC5_KS1(13))
T18904(KBC5_KS1(14))
T18905(KBC5_KS1(15))
T18906(KBC5_KS1(16))
T18907(KBC5_KS1(17))
T18908(KBC5_KS1(18))
T18909(KBC5_KS1(19))
T18910(KBC5_KS1(20))
T18911(KBC5_KS1(21))
T18912(KBC5_KS1(22))
T18913(KBC5_KS1(23))
T18914(KBC5_KS1(24))
T18915(KBC5_KS1(25))
T18916(KBC5_KS1(26))
T18917(KBC5_KS1(27))
T18918(KBC5_KS1(28))
T18919(KBC5_KS1(29))
T18920(KBC5_KS1(30))
T18921(KBC5_KS1(31))
T18922(KBC5_KS1(32))
T18923(KBC5_KS1(33))
T18924(KBC5_KS1(34))
T18925(KBC5_KS1(35))
T18926(KBC5_KS1(36))
T18927(KBC5_KS1(37))
T18928(KBC5_KS1(38))
T18929(KBC5_KS1(39))
T18930(KBC5_KS1(40))
T18931(KBC5_KS1(41))
T18932(KBC5_KS1(42))
T18933(KBC5_KS1(43))
T18934(KBC5_KS1(44))
T18935(KBC5_KS1(45))
T18936(KBC5_KS1(46))
T18937(KBC5_KS1(47))
T18938(KBC5_KS1(48))
T18939(KBC5_KS1(49))
T18940(KBC5_KS1(50))
T18941(KBC5_KS1(51))
T18942(KBC5_KS1(52))
T18943(KBC5_KS1(53))
T18944(KBC5_KS1(54))
T18945(KBC5_KS1(55))
T18946(KBC5_KS1(56))
T18947(KBC5_KS1(57))
T18948(KBC5_KS1(58))
T18949(KBC5_KS1(59))
T18950(KBC5_KS1(60))
T18951(KBC5_KS1(61))
T18952(KBC5_KS1(62))
T18953(KBC5_KS1(63))
T18954(KBC5_KS1(64))
T18955(KBC5_KS1(65))
T18956(KBC5_KS1(66))
T18957(KBC5_KS1(67))
T18958(KBC5_KS1(68))
T18959(KBC5_KS1(69))
T18960(KBC5_KS1(70))
T18961(KBC5_KS1(71))
T18962(KBC5_KS1(72))
T18963(KBC5_KS1(73))
T18964(KBC5_KS1(74))
T18965(KBC5_KS1(75))
T18966(KBC5_KS1(76))
T18967(KBC5_KS1(77))
T18968(KBC5_KS1(78))
T18969(KBC5_KS1(79))
T18970(KBC5_KS1(80))
T18971(KBC5_KS1(81))
T18972(KBC5_KS1(82))
T18973(KBC5_KS1(83))
T18974(KBC5_KS1(84))
T18975(KBC5_KS1(85))
T18976(KBC5_KS1(86))
T18977(KBC5_KS1(87))
T18978(KBC5_KS1(88))
T18979(KBC5_KS1(89))
T18980(KBC5_KS1(90))
T18981(KBC5_KS1(91))
T18982(KBC5_KS1(92))
T18983(KBC5_KS1(93))
T18984(KBC5_KS1(94))
T18985(KBC5_KS1(95))
T18986(KBC5_KS1(96))
T18987(KBC5_KS1(97))
T18988(KBC5_KS1(98))
T18989(KBC5_KS1(99))
T18990(KBC5_KS1(100))
T18991(KBC5_KS1(101))
T18992(KBC5_KS1(102))
T18993(KBC5_KS1(103))
T18994(KBC5_KS1(104))
T18995(KBC5_KS1(105))
T18996(KBC5_KS1(106))
T18997(KBC5_KS1(107))
T18998(KBC5_KS1(108))
T18999(KBC5_KS1(109))
T19000(KBC5_KS1(110))
T19001(KBC5_KS1(111))
T19002(KBC5_KS1(112))
T19003(KBC5_KS1(113))
T19004(KBC5_KS1(114))
T19005(KBC5_KS1(115))
T19006(KBC5_KS1(116))
T19007(KBC5_KS1(117))
T19008(KBC5_KS1(118))
T19009(KBC5_KS1(119))
T19010(KBC5_KS1(120))
T19011(KBC5_KS1(121))
T19012(KBC5_KS1(122))
T19013(KBC5_KS1(123))
T19014(KBC5_KS1(124))
T19015(KBC5_KS1(125))
T19016(KBC5_KS1(126))
T19017(KBC5_KS1(127))
T19018(KBC5_KS1(128))
T19019(KBC5_KS1(129))
T19020(KBC5_KS1(130))
T19021(KBC5_KS1(131))
T19022(KBC5_KS1(132))
T19023(KBC5_KS1(133))
T19024(KBC5_KS1(134))
T19025(KBC5_KS1(135))
T19026(KBC5_KS1(136))
T19027(KBC5_KS1(137))
T19028(KBC5_KS1(138))
T19029(KBC5_KS1(139))
T19030(KBC5_KS1(140))
T19031(KBC5_KS1(141))
T19032(KBC5_KS1(142))
T19033(KBC5_KS1(143))
T19034(KBC5_KS1(144))
T19035(KBC5_KS1(145))
T19036(KBC5_KS1(146))
T19037(KBC5_KS1(147))
T19038(KBC5_KS1(148))
T19039(KBC5_KS1(149))
T19040(KBC5_KS1(150))
T19041(KBC5_KS1(151))
T19042(KBC5_KS1(152))
T19043(KBC5_KS1(153))
T19044(KBC5_KS1(154))
T19045(KBC5_KS1(155))
T19046(KBC5_KS1(156))
T19047(KBC5_KS1(157))
T19048(KBC5_KS1(158))
T19049(KBC5_KS1(159))
T19050(KBC5_KS1(160))
T19051(KBC5_KS1(161))
T19052(KBC5_KS1(162))
T19053(KBC5_KS1(163))
T19054(KBC5_KS1(164))
T19055(KBC5_KS1(165))
T19056(KBC5_KS1(166))
T19057(KBC5_KS1(167))
T19058(KBC5_KS1(168))
T19059(KBC5_KS1(169))
T19060(KBC5_KS1(170))
T19061(KBC5_KS1(171))
T19062(KBC5_KS1(172))
T19063(KBC5_KS1(173))
T19064(KBC5_KS1(174))
T19065(KBC5_KS1(175))
T19066(KBC5_KS1(176))
T19067(KBC5_KS1(177))
T19068(KBC5_KS1(178))
T19069(KBC5_KS1(179))
T19070(KBC5_KS1(180))
T19071(KBC5_KS1(181))
T19072(KBC5_KS1(182))
T19073(KBC5_KS1(183))
T19074(KBC5_KS1(184))
T19075(KBC5_KS1(185))
T19076(KBC5_KS1(186))
T19077(KBC5_KS1(187))
T19078(KBC5_KS1(188))
T19079(KBC5_KS1(189))
T19080(KBC5_KS1(190))
T19081(KBC5_KS1(191))
T19082(KBC5_KS1(192))
T19083(KBC5_KS1(193))
T19084(KBC5_KS1(194))
T19085(KBC5_KS1(195))
T19086(KBC5_KS1(196))
T19087(KBC5_KS1(197))
T19088(KBC5_KS1(198))
T19089(KBC5_KS1(199))
T19090(KBC5_KS1(200))
T19091(KBC5_KS1(201))
T19092(KBC5_KS1(202))
T

TP190205@SC486_EN_PSV
 TP190206@SC486_FB
 TP190208@SMB3_CLK
 TP190209@SMB3_DATA
 TP190300@SPI2_CLK
 TP190301@SPI2_CS#
 TP190302@SPI2_CS#_MISO
 TP190303@SPI2_CS#_MOSI
 TP190304@STRAP_BIOSROM
 TP190305@STRAP_BIOSROM#
 TP190306@STRAP_USB4#
 TP190307@TRMR3_ALERT#
 TP190308@TRMR3_ALERT#_GREEN
 TP190400@PEG3_CRT_HSYNC
 TP190401@PEG3_CRT_RED
 TP190402@PEG3_CRT_VSYNC
 TP190403@PEG3_CCD_BKLT_EN
 TP190404@PEG3_CCD_BR1
 TP190405@PEG3_LCD_VDDON
 TP190406@PEG3_CRT_BLUE
 TP190407@PEG3_CRT_DDCCLK
 TP190408@PEG3_CCD_CDCAATA
 TP190409@ODDS_0(1)
 TP190409@ODDS_0(2)
 TP190500@ODDS_0(3)
 TP190501@ODDS_0(4)
 TP190502@ODDS_0(5)
 TP190503@ODDS_0(2)
 TP190504@ODDS_0(3)
 TP190505@ODDS_0(4)
 TP190506@ODDS_0(5)
 TP190507@ODDS_0(6)
 TP190508@ODDS_0(7)
 TP190509@ODDS_0(8)
 TP190600@ODDS_0(9)
 TP190601@ODDS_0(10)
 TP190602@ODDS_0(11)
 TP190603@ODDS_0(12)
 TP190604@ODDS_0(13)
 TP190605@ODDS_0(14)
 TP190606@ODDS_0(15)
 TP190607@P1_2V_PWRGD
 TP190608@P2_5V_PWRGD
 TP190609@P3_3V_CLKRUN#
 TP190700@ODDS_0(16)
 TP190701@ODDS_0(17)
 TP190702@ODDS_0(18)
 TP190703@ODDS_0(19)
 TP190704@ODDS_0(20)
 TP190705@ODDS_0(21)
 TP190706@ODDS_0(22)
 TP190707@ODDS_0(23)
 TP190708@_BUTTON
 TP190709@_BUTTON#
 TP190803@AGNO_CHG

TP19092 ○ VCCP3_PWRGD
TP19093 ○ VGA3_VOLTAGE_ID
TP19094 ○ VGA5-DDCC
TP19095 ○ VGA5-DDCD
TP19096 ○ VRM1-DPRSTP#
TP19097 ○ VRM3-CPU_PWRGD
TP19091 ○ WLN_LED#
TP19090 ○ AD_DC

TP19159 P1.8V_AUX
TP19160 P1.8V_GFX
TP19167 P12.0V_ALW
TP19168 CP2.5V
TP19175 CP2.5V_LAN
TP19176 CP2.5V
TP19183 CP3.3V_AUX
TP19187 CP3.3V_AUX_EXP
TP19191 P1.2V

TP19199 P1.2V_AUX
TP19200 P1.2V_LAN
TP19207 CP1.2V_PEG
TP19208 CP1.2V_PEG
TP19215 CP1.5V_EXP
TP19216 P1.8V
TP19227 CP3.3V
TP19228 INV_VDD3V
TP19235 CLCD_VDD3V
TP19239 CLCD_VDD3V
TP19240 MEM1_REF
TP19247 MICOM_P3.3V
TP19248 CP0.9V
TP19275 CG_CPU
TP19276 CG_D0R
TP19280 C0H0_REF
TP19267 C0FX_CORE
TP19268 CG_AUD

TP19283 OG_GFX
TP19284 OG_P1.2V