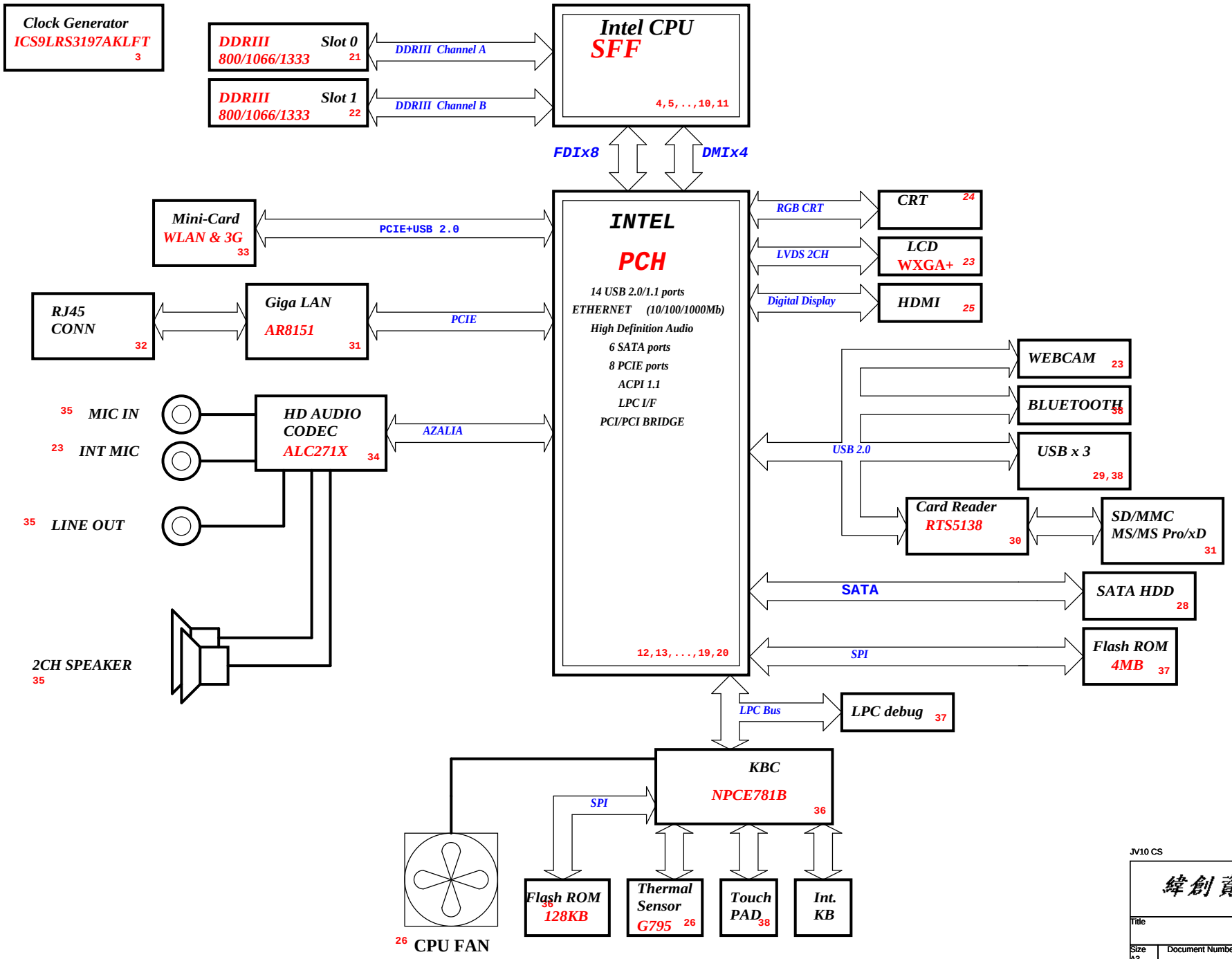
JV10-CS Block Diagram

Project code:91.4GS01.001
PCB P/N :48.4GS01.0SA
REVISION :09918-1



SYSTEM DC/DC RT8223	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 42

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 43

SYSTEM DC/DC RT8209B	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 44

SYSTEM DC/DC RT9026	
INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 43

CPU DC/DC TPS51611	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 41

INTERSIL CHARGER ISL88731A	
INPUTS	OUTPUTS
DCBATOUT	BT+ 45

PCB STACKUP

TOP
Power
S
S
GND
BOTTOM

JV10 CS

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Title: Block Diagram

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

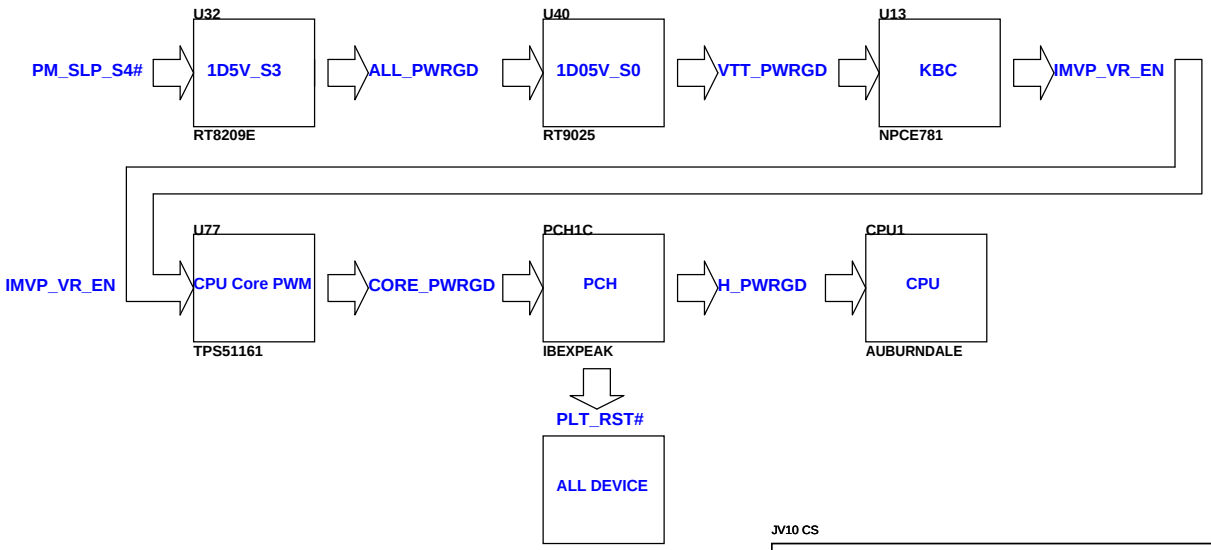
PCIE Routing

LANE1	LAN
LANE2	MiniCard1

USB Table

Pair	Device
0	USB3
1	USB2
2	NC
3	MINICARD1
4	WECAM
5	NC
6	NC
7	NC
8	NC
9	USB1(HS)
10	NC
11	Blue Tooth
12	MINIC2
13	Cardreader

Power Sequence



JV10 CS

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Title: *Table of Content*

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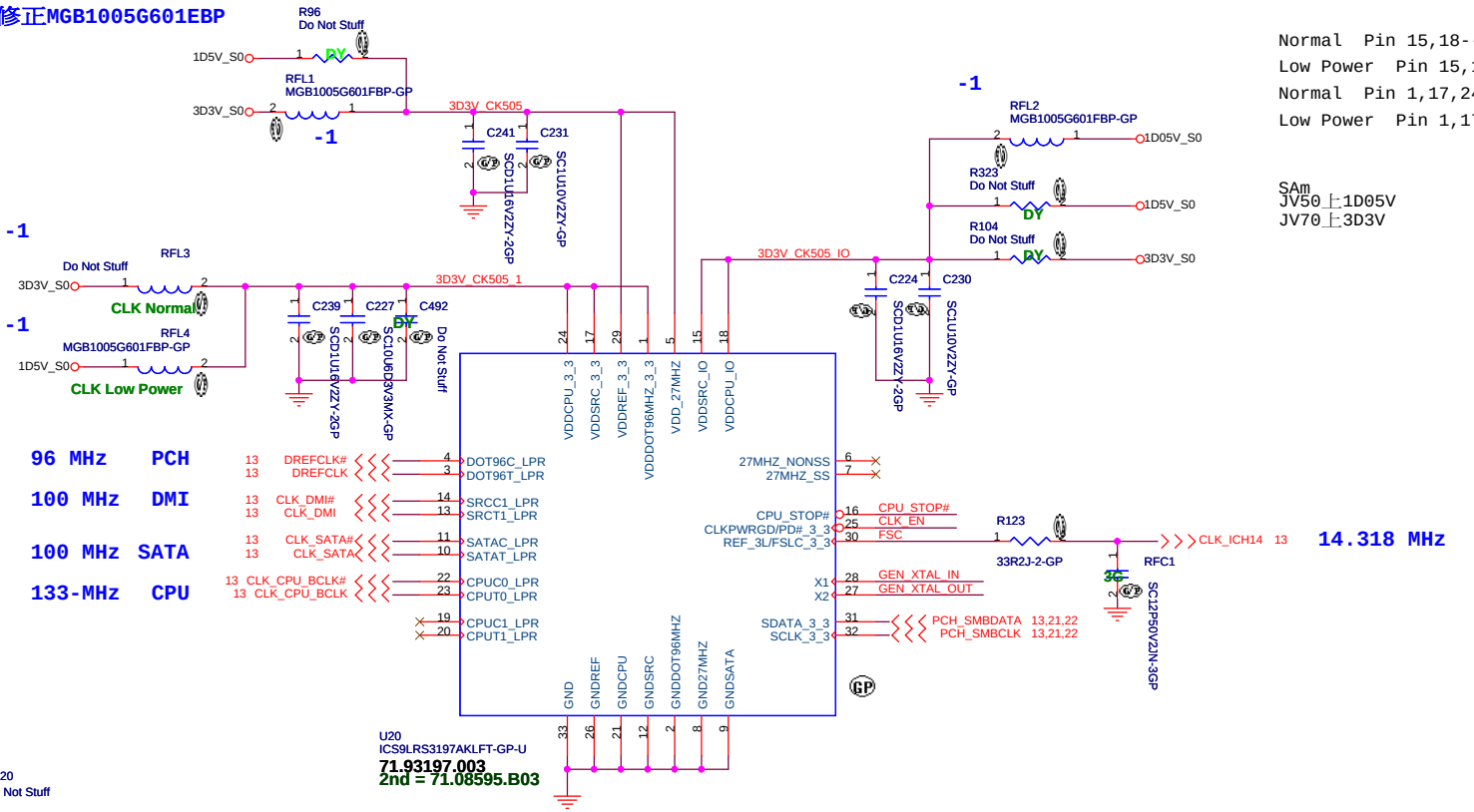
RFL1~4 將來EC 修正MGB1005G601EBP
料號申請中
68.00373.001

Normal Pin 15,18----3.3V/1.05V
Low Power Pin 15,18---1.5V/1.05V
Normal Pin 1,17,24---3.3V/1.05V
Low Power Pin 1,17,24---1.5V/1.05V

SAm
JV50上1D05V
JV70上3D3V



CLK Lower Power ICS:71.93197.B03,SILEGO:71.08595.003

FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: Clock Generator

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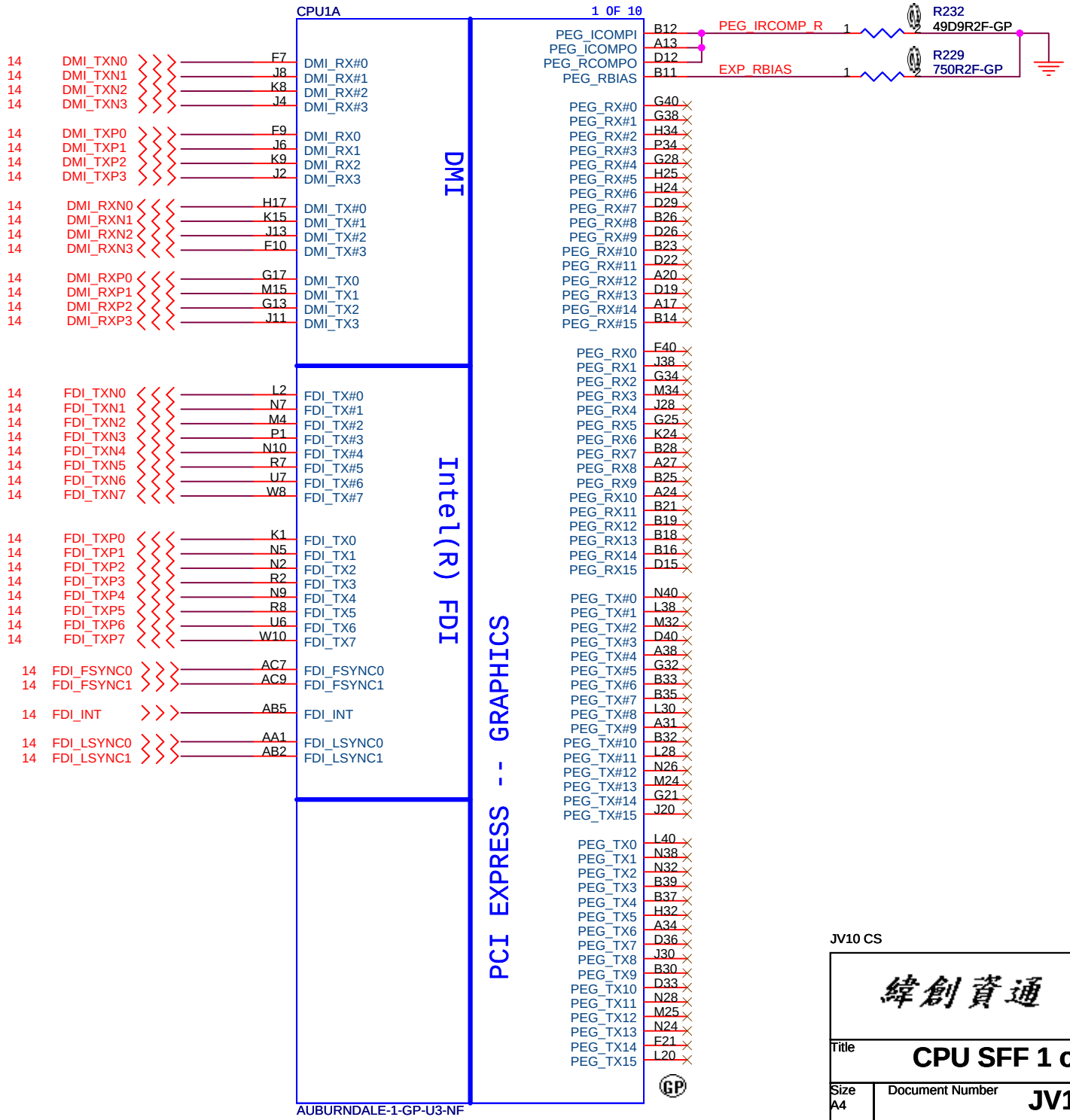

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Title: **CPU SFF 1 of 8(DMI/FDI/PEG)**

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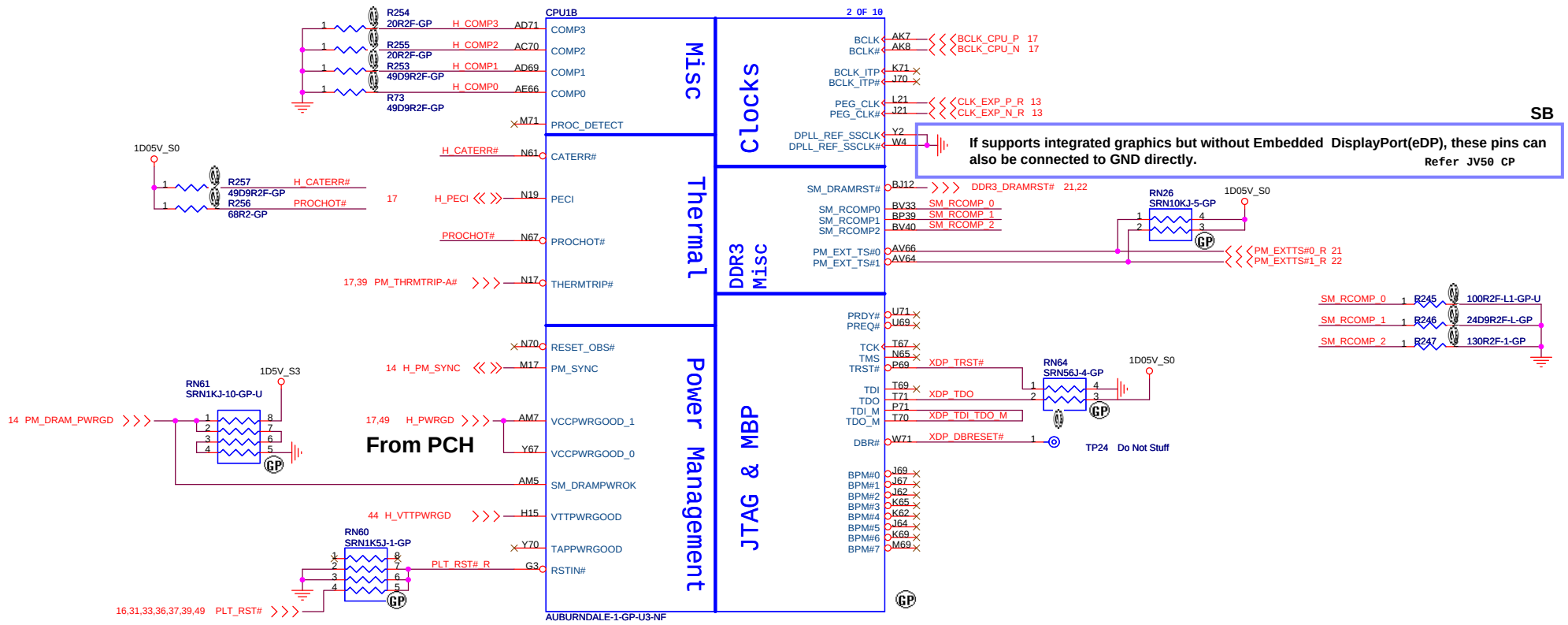

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Title	CPU SFF 2 of 8(CLK/Thermal)	
Size: Custom	Document Number: JV10-CS	Rev: -1
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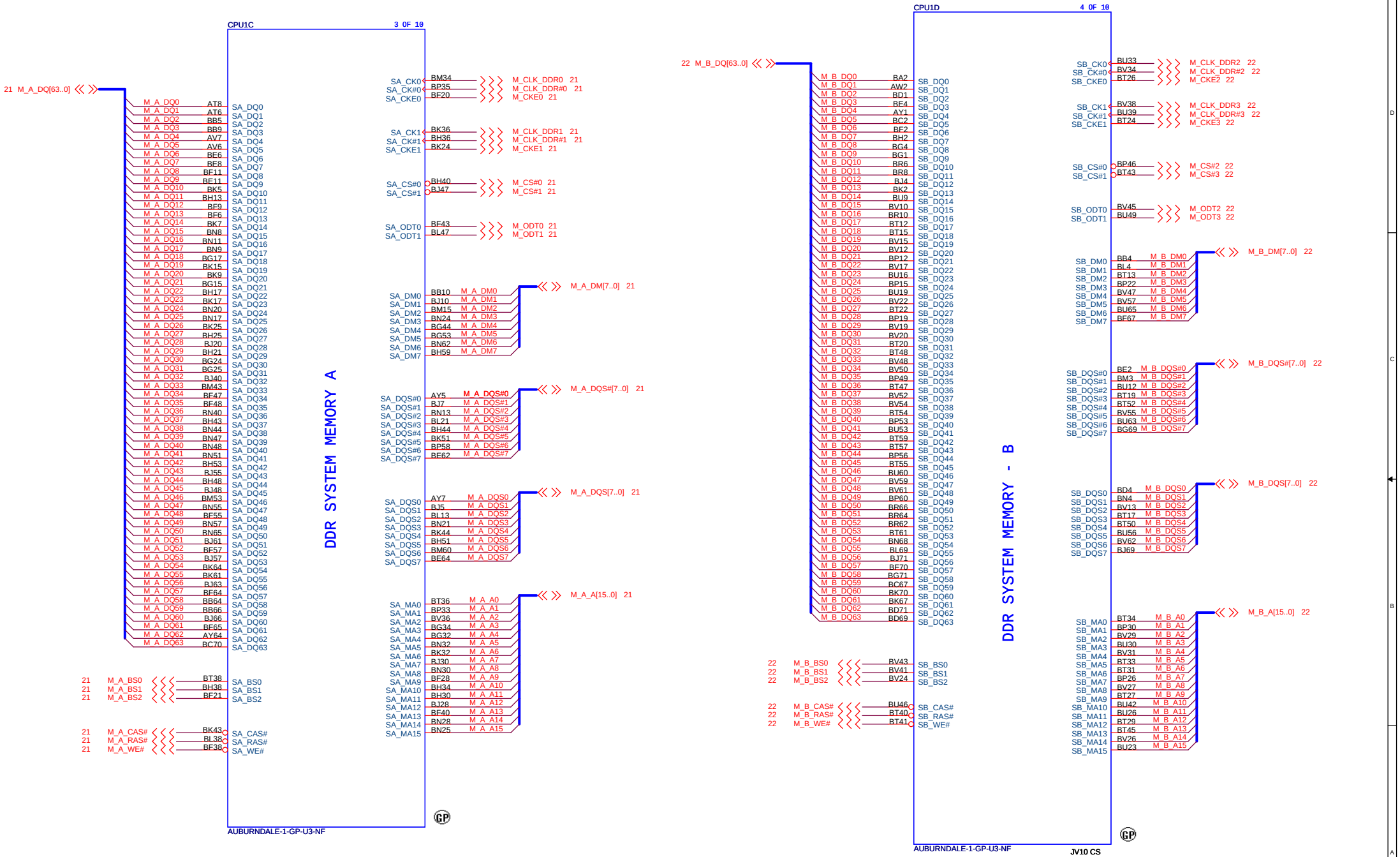

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Title	**CPU SFF 3 of 8(DDR)**	
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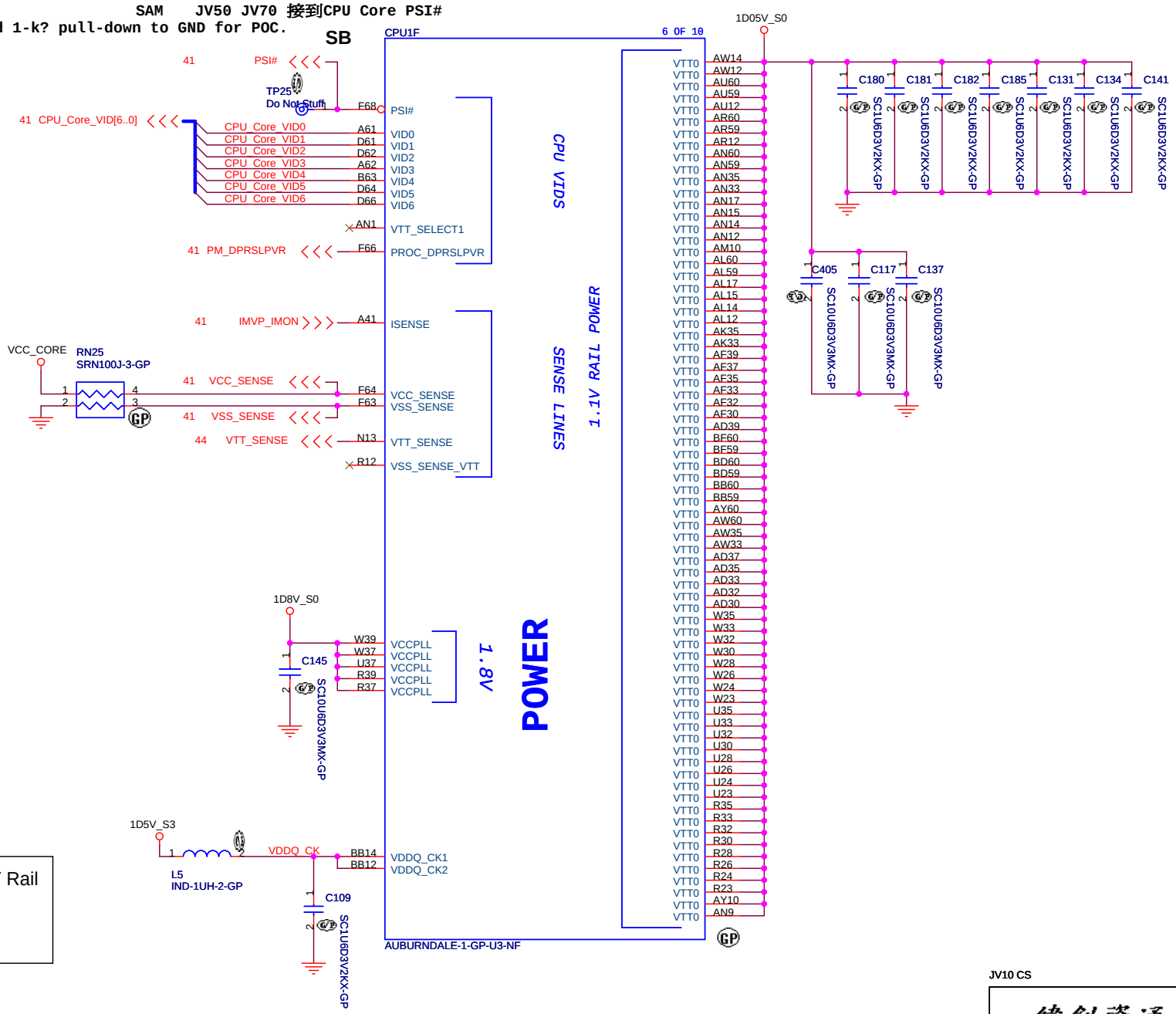
check list
1-k? pull-up to VTT and 1-k? pull-down to GND for POC.
1D05V_VTT

SAM JV50 JV70 接到CPU Core PSI#



Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

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Title: CPU SFF 4 of 8(POWER/VTT)

Size	Document Number	Rev
Custom	JV10-CS	-1

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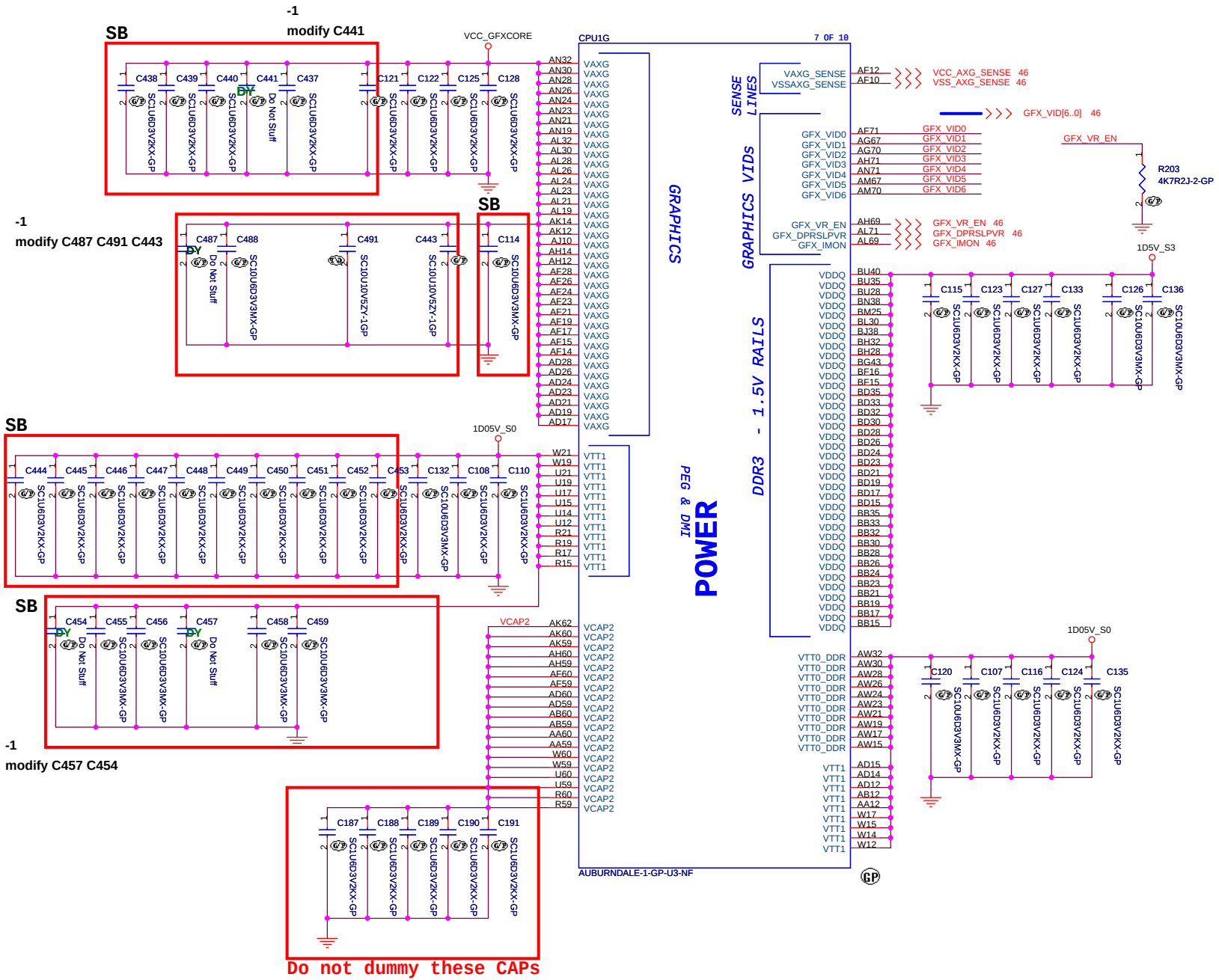

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Title	CPU SFF 5 of 8(PWR/DDR/GFX/)	
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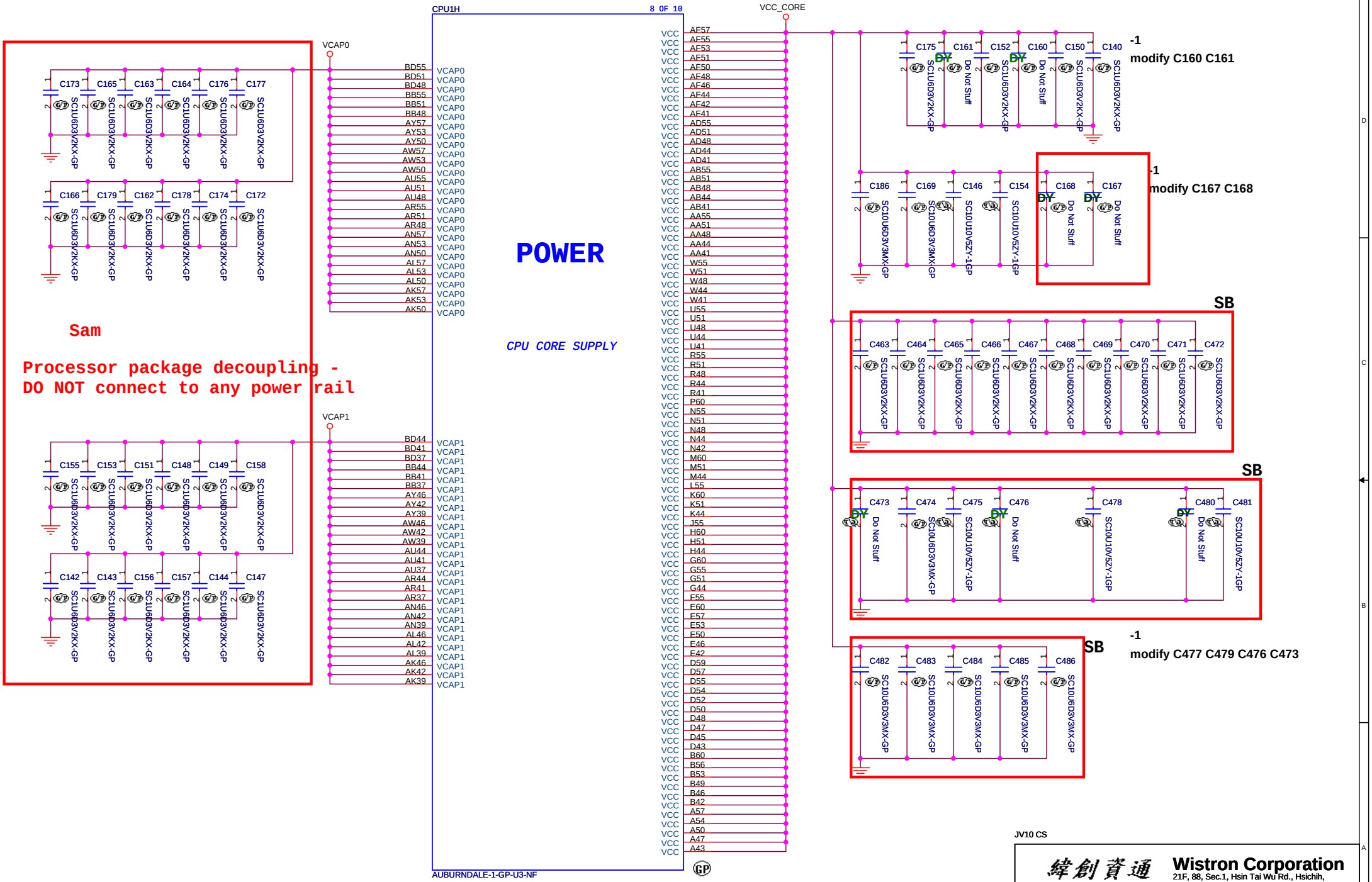

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Title: CPU SFF 6 of 8(CPUCORE)

Size: Custom | Document Number: JV10-CS | Rev: -1

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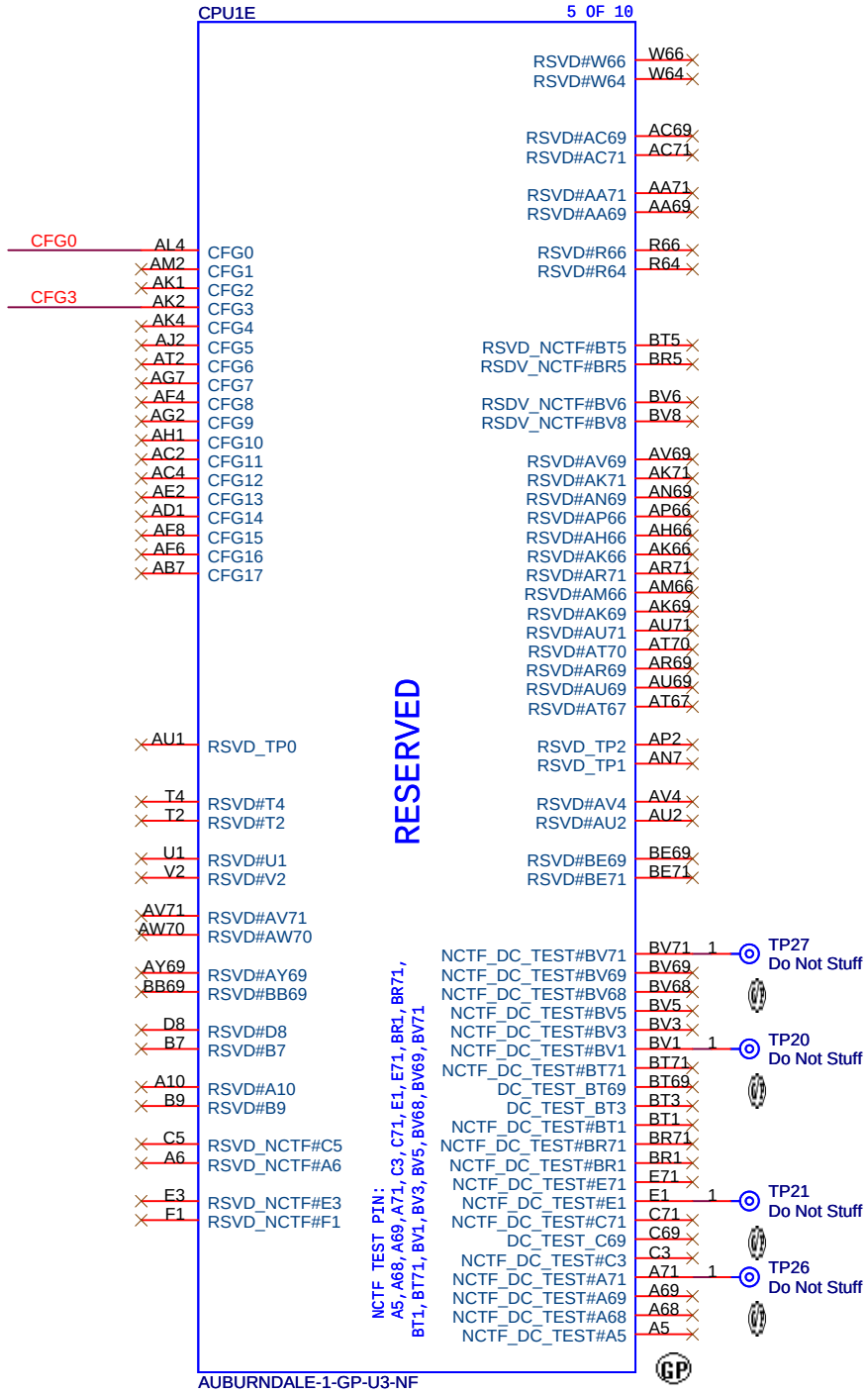

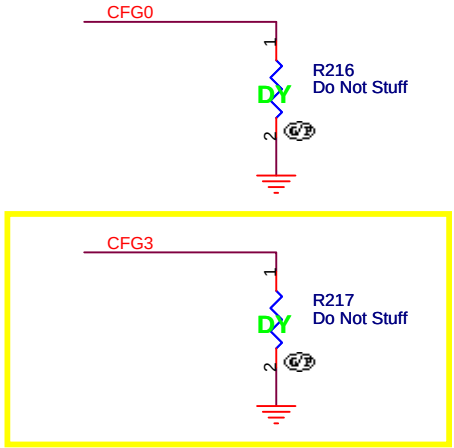

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

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Title: **CPU SFF 7 of 8(RESERVED)**

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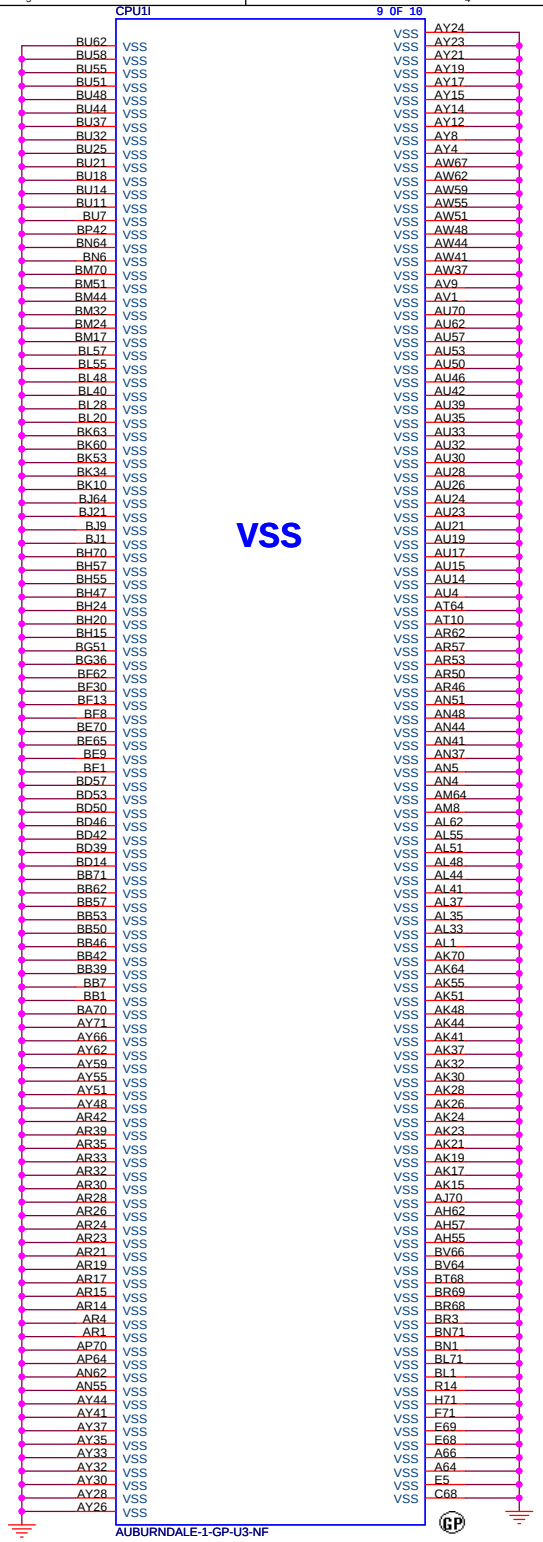

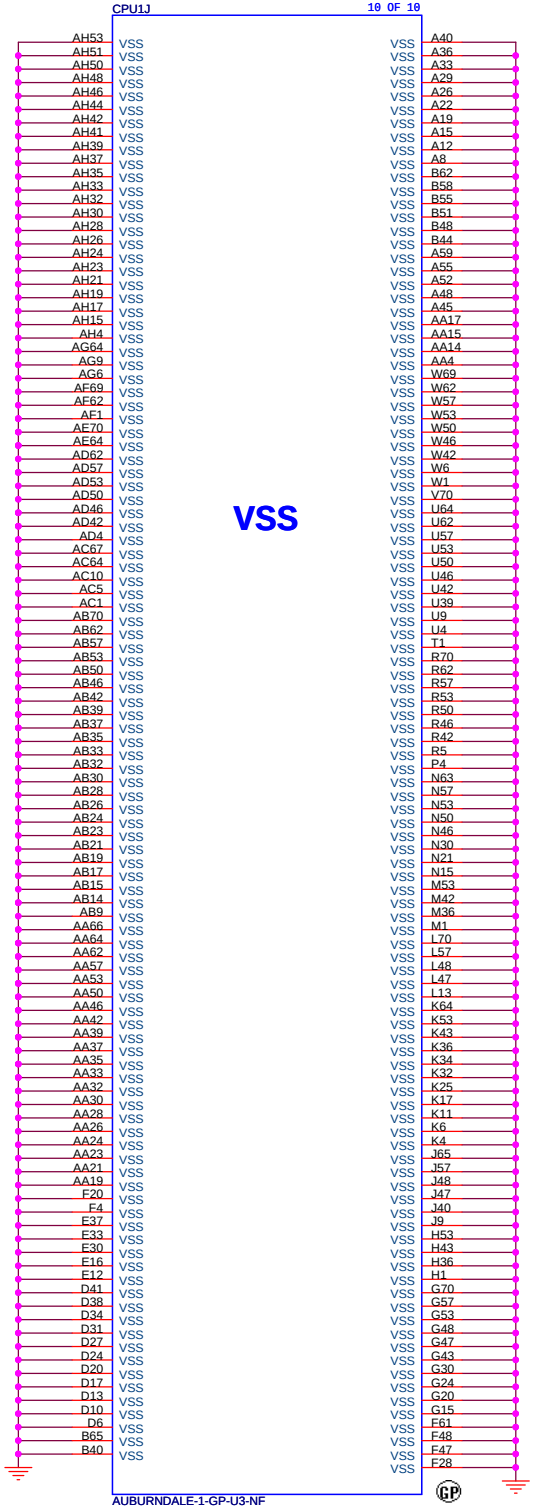

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Title	**CPU SFF 8 of 8(VSS)**	
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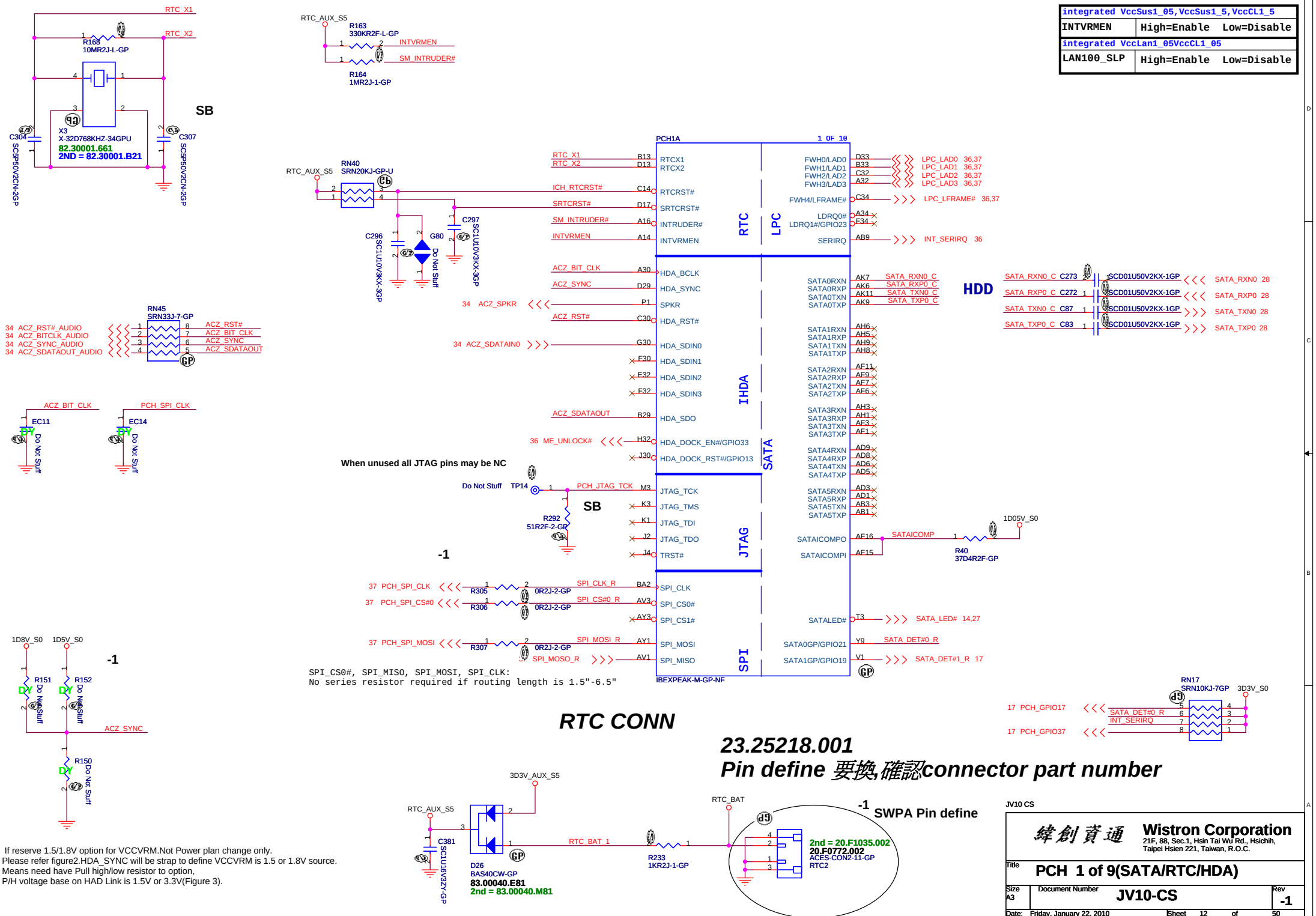
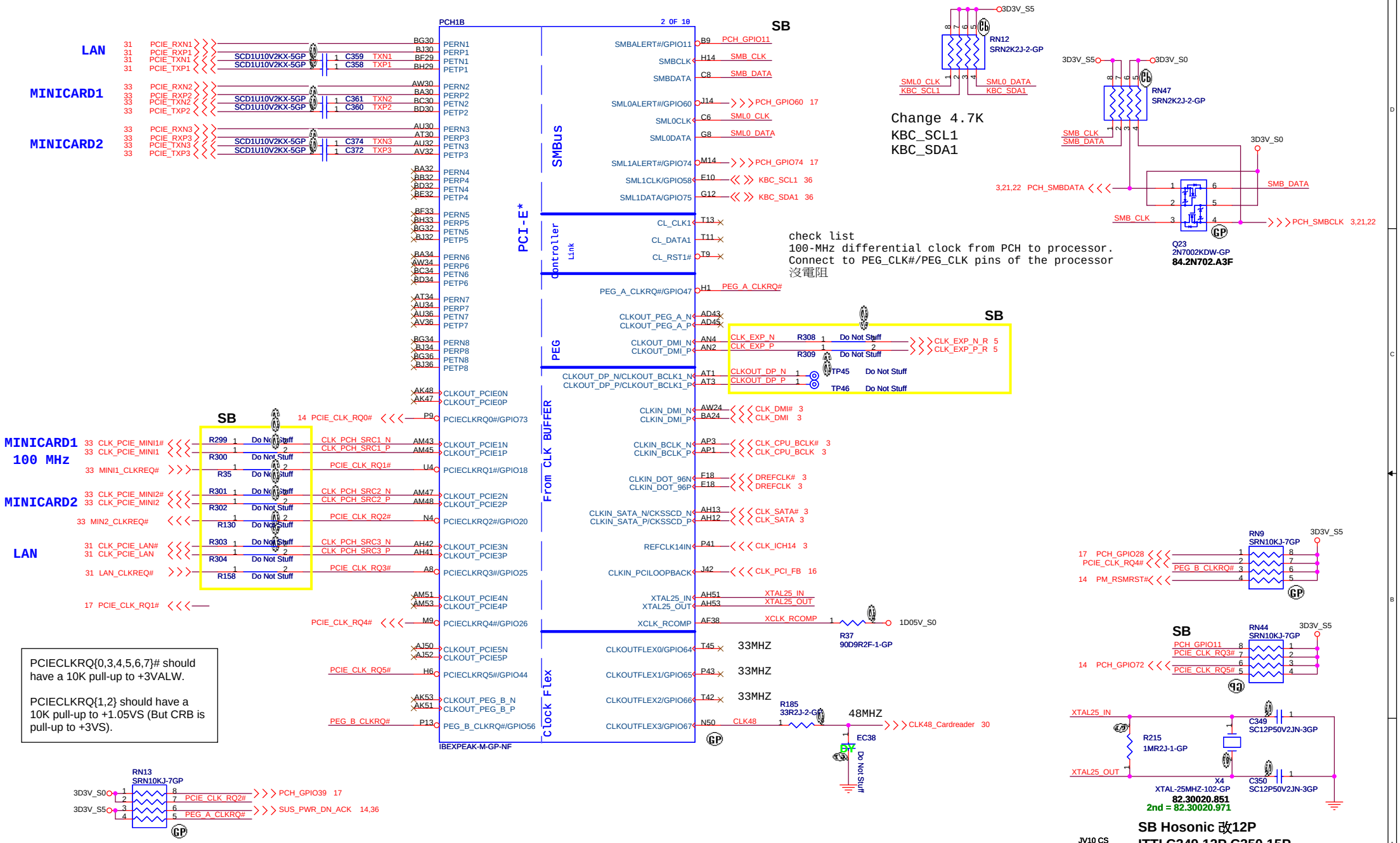
integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable




PCH1B
2 OF 10
SB
LAN
MINICARD1
MINICARD2
PCIE_RXN1
PCIE_RXP1
PCIE_TXN1
PCIE_TXP1
PCIE_RXN2
PCIE_RXP2
PCIE_TXN2
PCIE_TXP2
PCIE_RXN3
PCIE_RXP3
PCIE_TXN3
PCIE_TXP3
SCD1U10V2KX-5GP
C359
C358
C361
C360
C374
C372
TXN1
TXP1
TXN2
TXP2
TXN3
TXP3
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
PCI-E*
SMBus
Controller
Link
PEG
From CLK BUFFER
Clock Flex
SMBALERT#/GPIO11
SMBCLK
SMBDATA
SML0ALERT#/GPIO60
SML0CLK
SML0DATA
SML1ALERT#/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
PCH_GPIO11
SMB_CLK
SMB_DATA
PCH_GPIO60
SML0_CLK
SML0_DATA
PCH_GPIO74
KBC_SCL1
KBC_SDA1
CL_CLK1
CL_DATA1
CL_RST1#
PEG_A_CLKRQ#/GPIO47
PEG_A_CLKRQ#
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N/CLKOUT_BCLK1_N
CLKOUT_DP_P/CLKOUT_BCLK1_P
CLK_EXP_N
CLK_EXP_P
CLK_EXP_N_R
CLK_EXP_P_R
R308
R309
Do Not Stuff
TP45
TP46
CLKOUT_PCIE0N
CLKOUT_PCIE0P
PCIECLKRQ0#/GPIO73
PCIE_CLK_RQ0#
CLKOUT_PCIE1N
CLKOUT_PCIE1P
PCIECLKRQ1#/GPIO18
PCIE_CLK_RQ1#
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2#/GPIO20
PCIE_CLK_RQ2#
CLKOUT_PCIE3N
CLKOUT_PCIE3P
PCIECLKRQ3#/GPIO25
PCIE_CLK_RQ3#
CLKOUT_PCIE4N
CLKOUT_PCIE4P
PCIECLKRQ4#/GPIO26
PCIE_CLK_RQ4#
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5#/GPIO44
PCIE_CLK_RQ5#
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ#/GPIO56
PEG_B_CLKRQ#
IBEXPEAK-M-GP-NF
CLKIN_DMI_N
CLKIN_DMI_P
CLK_DMI#
CLK_DMI
CLKIN_BCLK_N
CLKIN_BCLK_P
CLK_CPU_BCLK#
CLK_CPU_BCLK
CLKIN_DOT_96N
CLKIN_DOT_96P
DREFCLK#
DREFCLK
CLKIN_SATA_N/CKSSCD_N
CLKIN_SATA_P/CKSSCD_P
CLK_SATA#
CLK_SATA
REFCLK14IN
CLK_ICH14
CLKIN_PCILOOPBACK
CLK_PCI_FB
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
R37
90D9R2F-1-GP
1D05V_S0
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
33MHZ
48MHZ
CLK48
R185
33R2J-2-GP
EC38
CLK48_Cardreader
MINICARD1 100 MHz
MINICARD2
LAN
CLK_PCIE_MINI1#
CLK_PCIE_MINI1
MINI1_CLKREQ#
CLK_PCIE_MINI2#
CLK_PCIE_MINI2
MIN2_CLKREQ#
CLK_PCIE_LAN#
CLK_PCIE_LAN
LAN_CLKREQ#
R299
R300
R35
R301
R302
R130
R303
R304
R158
CLK_PCH_SRC1_N
CLK_PCH_SRC1_P
CLK_PCH_SRC2_N
CLK_PCH_SRC2_P
CLK_PCH_SRC3_N
CLK_PCH_SRC3_P
PCIE_CLK_RQ1#
PCIE_CLK_RQ2#
PCIE_CLK_RQ3#
PCIE_CLK_RQ4#
PCIE_CLK_RQ5#
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
RN13
SRN10KJ-7GP
3D3V_S0
3D3V_S5
PCH_GPIO39
SUS_PWR_DN_ACK
PEG_A_CLKRQ#
EC7
EC5
EC12
RN12
SRN2K2J-2-GP
Change 4.7K
KBC_SCL1
KBC_SDA1
RN47
SRN2K2J-2-GP
PCH_SMBDATA
PCH_SMBCLK
Q23
2N7002KDW-GP
84.2N702.A3F
check list
100-MHz differential clock from PCH to processor.
Connect to PEG_CLK#/PEG_CLK pins of the processor
沒電阻
RN9
SRN10KJ-7GP
PCH_GPIO28
PEG_B_CLKRQ#
PM_RSMRST#
RN44
SRN10KJ-7GP
PCH_GPIO72
C349
SC12P50V2JN-3GP
R215
1MR2J-1-GP
X4
XTAL-25MHZ-102-GP
82.30020.851
2nd = 82.30020.971
C350
SC12P50V2JN-3GP
SB Hosonic 改12P
ITTI C349 12P,C350 15P
JV10 CS
Wistron Corporation
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Title
PCH 2 of 9(PCIE/CLK/SMB)
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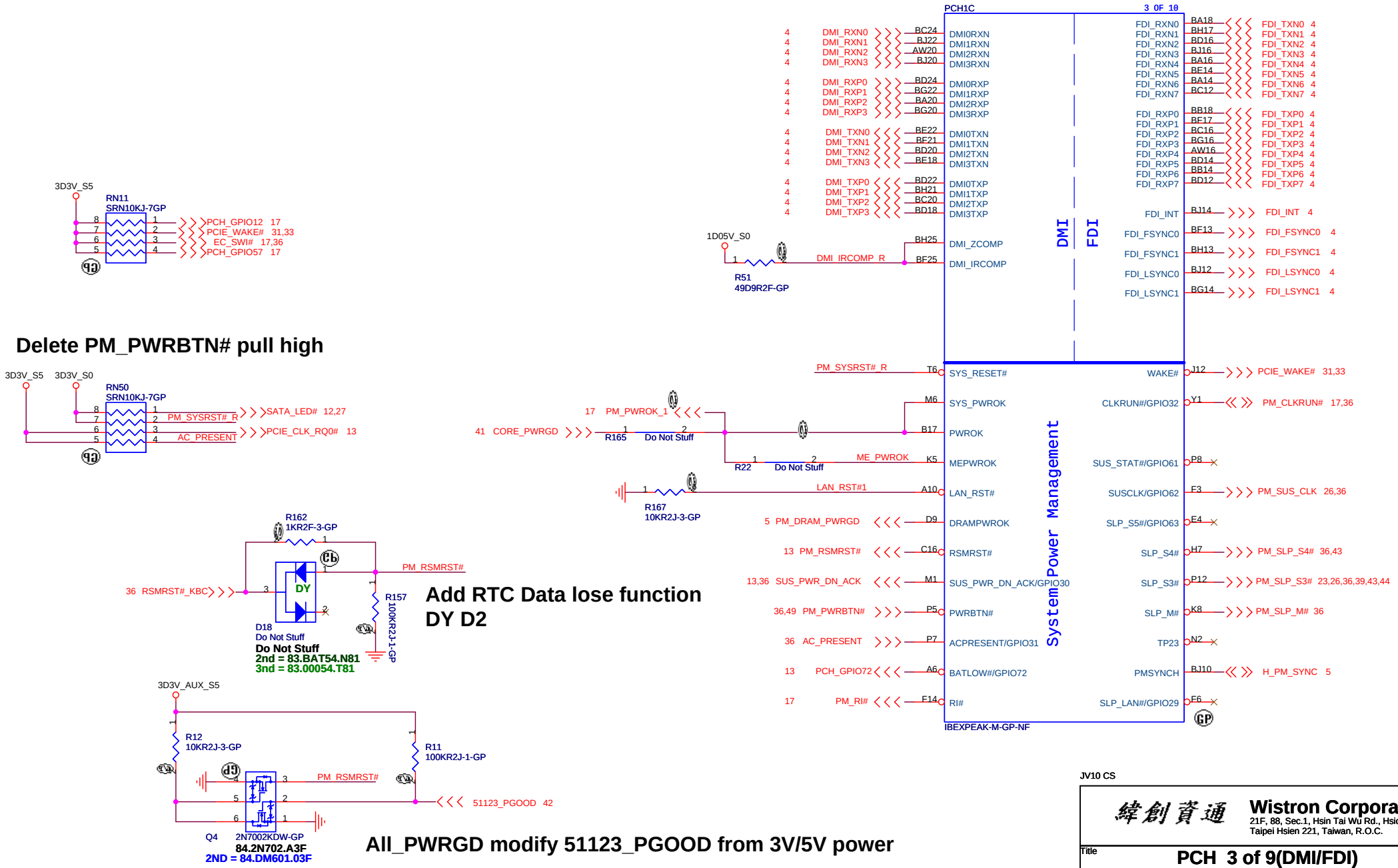

JV10 CS

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Title	PCH 3 of 9(DMI/FDI)		
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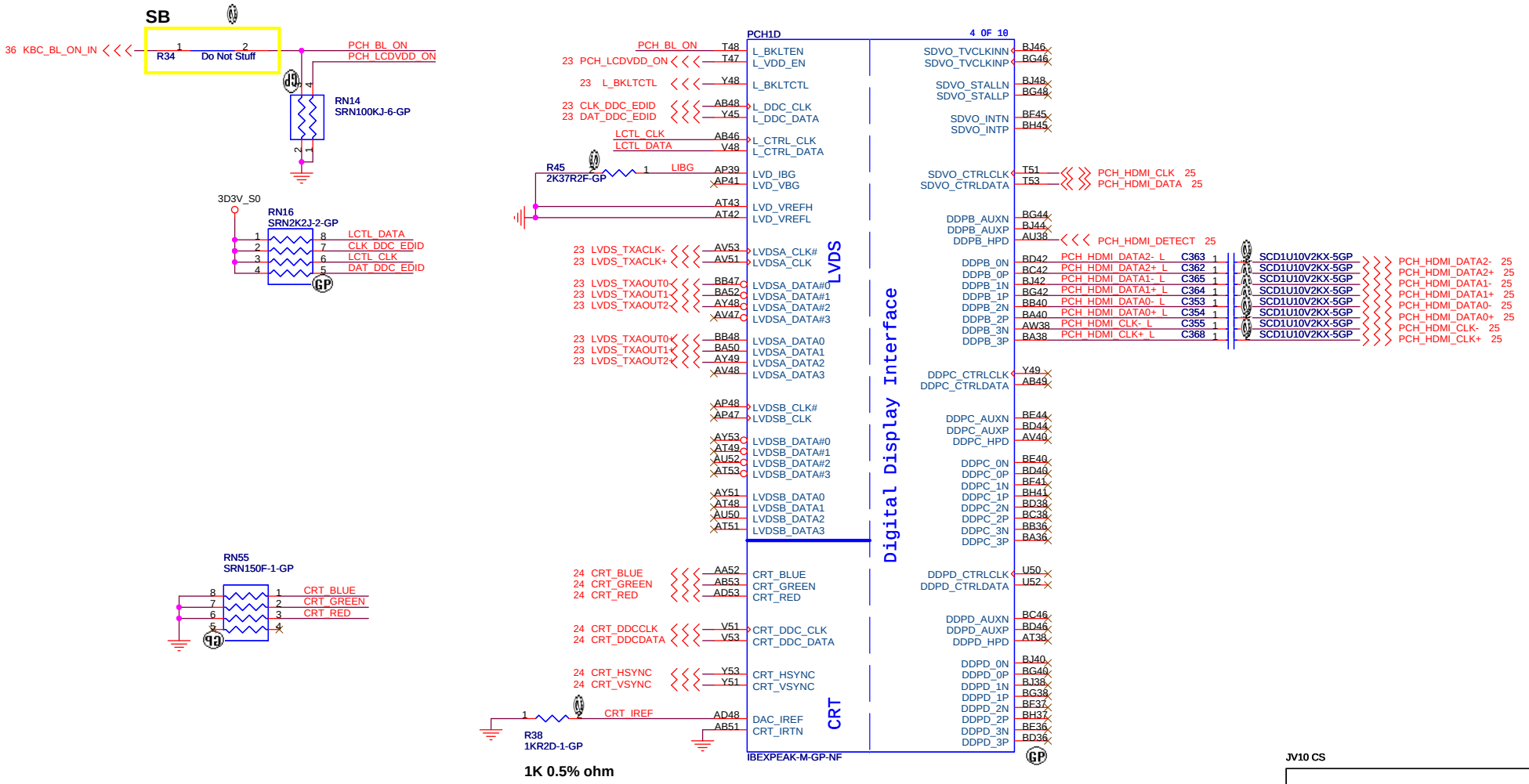
Panel backlight enable control for LVDS -
used to gate power into the backlight circuit



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Title: PCH 4 of 9(LVDS/CRT/DP)

Size	Document Number	Rev
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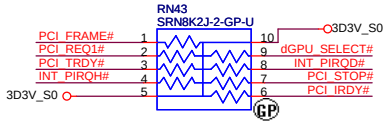
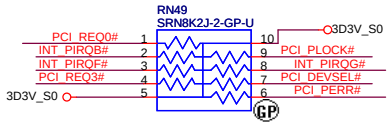
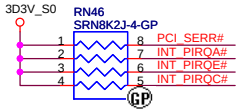
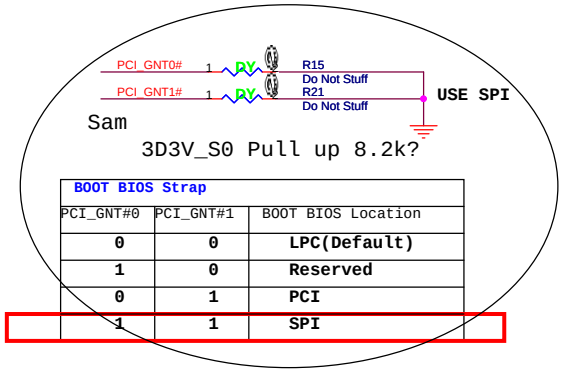


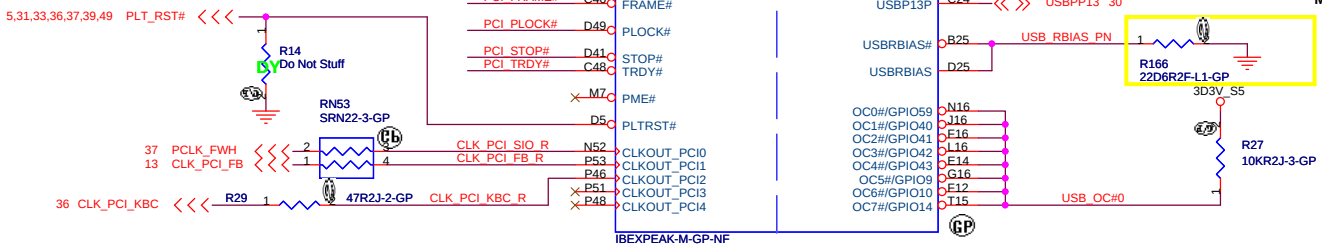




These pins are left as NC, because the function is disable.



BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

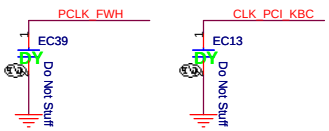


These pins are left as NC, because the function is disable.

USB Table

Pair	Device
0	USB3
1	USB2
2	NC
3	MINICARD1
4	WECAM
5	NC
6	NC
7	NC
8	3G
9	USB1(HS)
10	NC
11	Blue Tooth
12	MINIC2(3G)
13	Cardreader

SB
Modify SIV USB report



JV10 CS

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 5 of 9(PCI/USB)

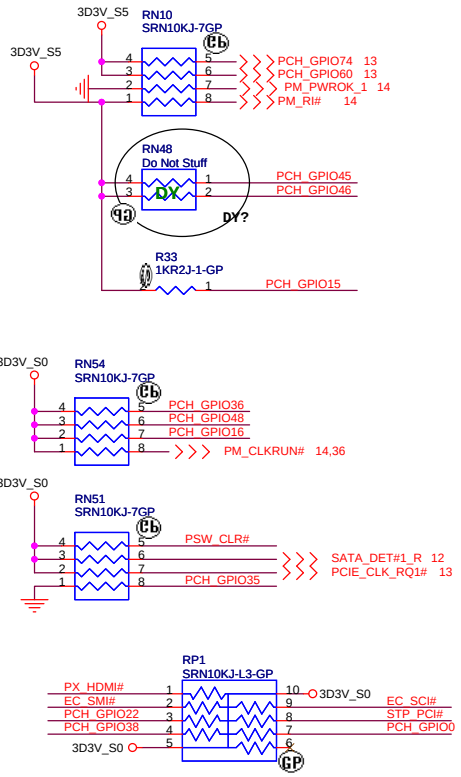
Size: A3 | Document Number: JV10-CS | Rev: -1

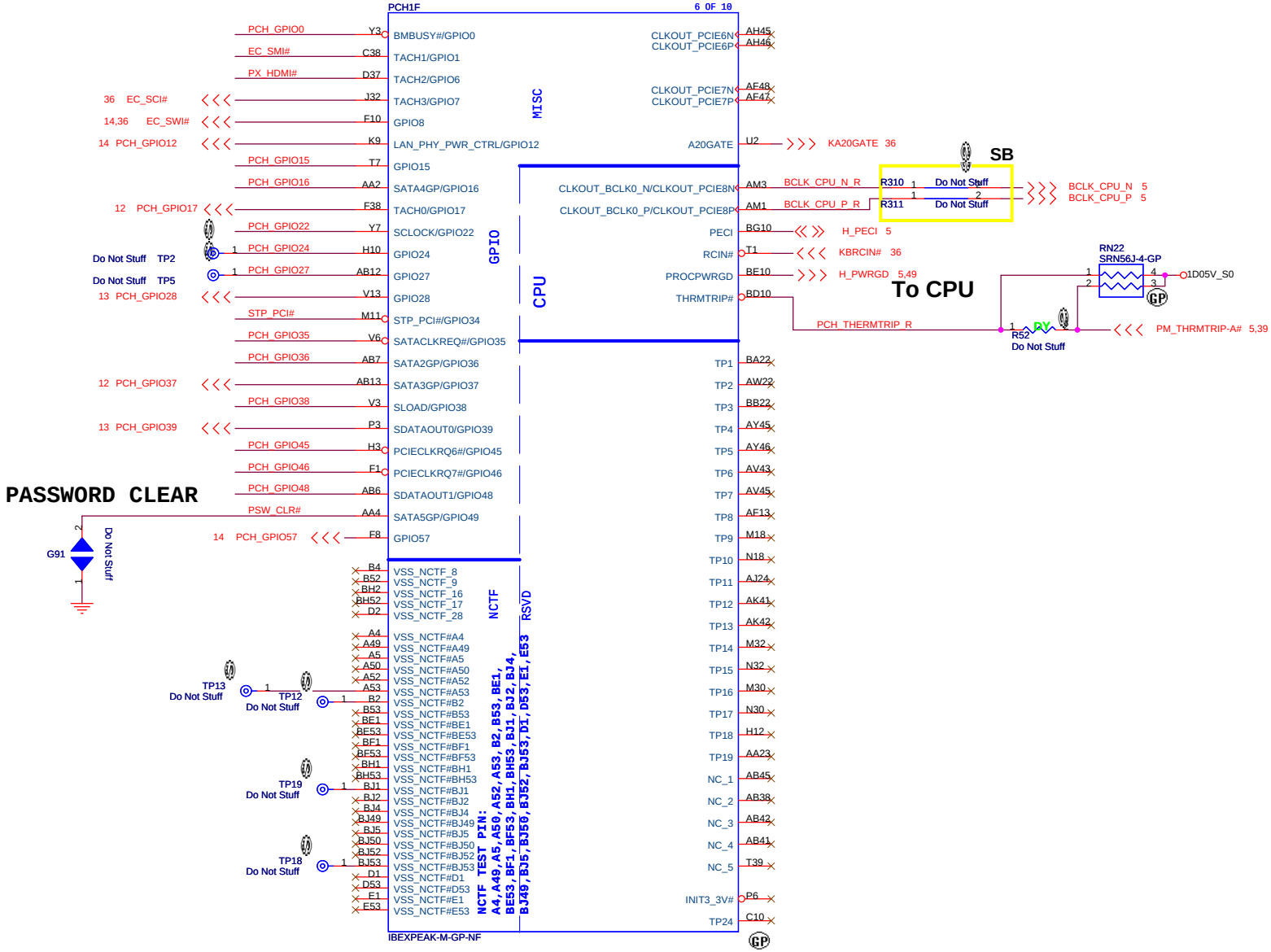
Date: Friday, January 22, 2010 | Sheet 16 of 50

GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

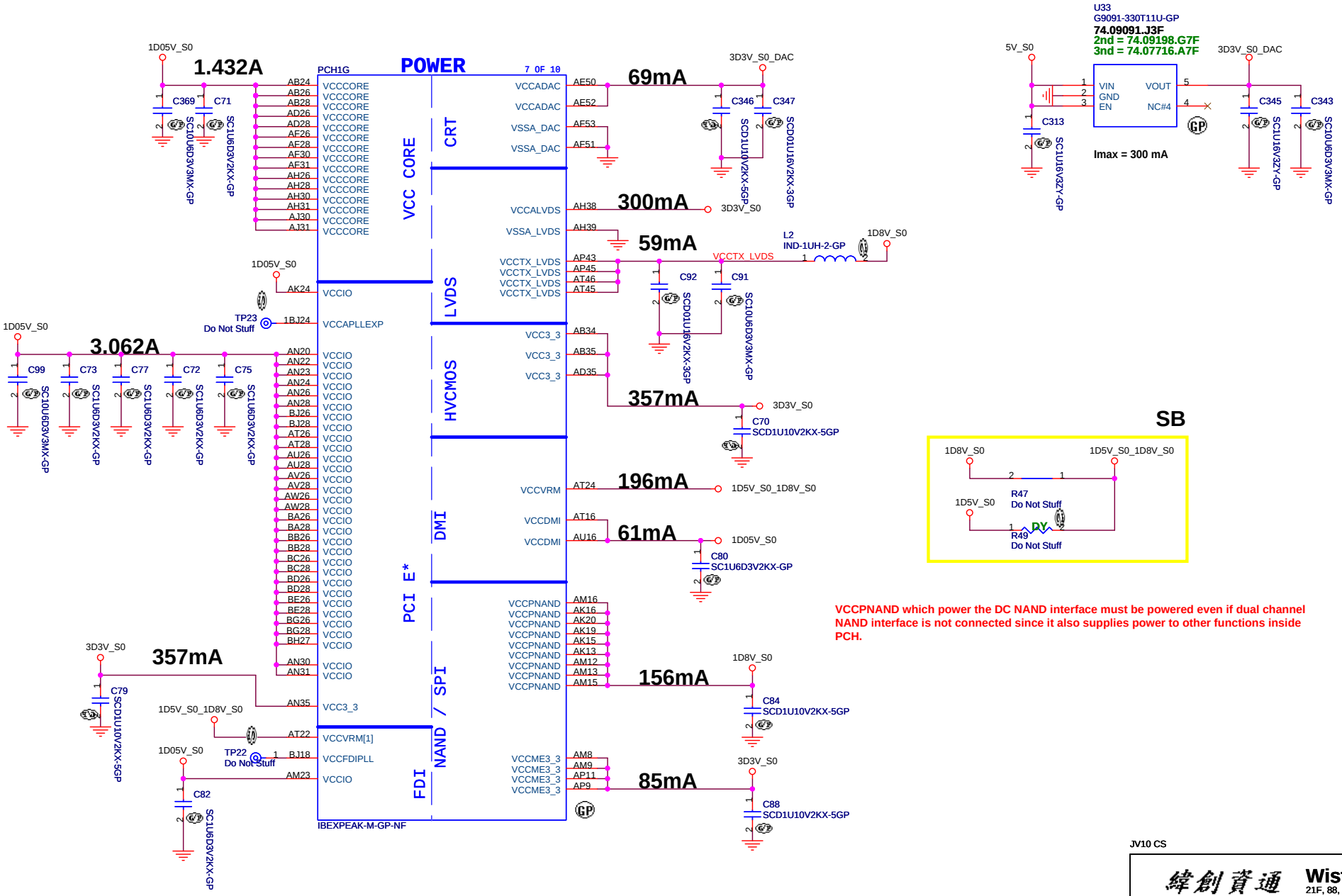
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.





JV10 CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH 6 of 9(GPIO/RSVD)	
Size A3	Document Number JV10-CS	Rev -1
Date: Friday, January 22, 2010	Sheet 17 of 50	



VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

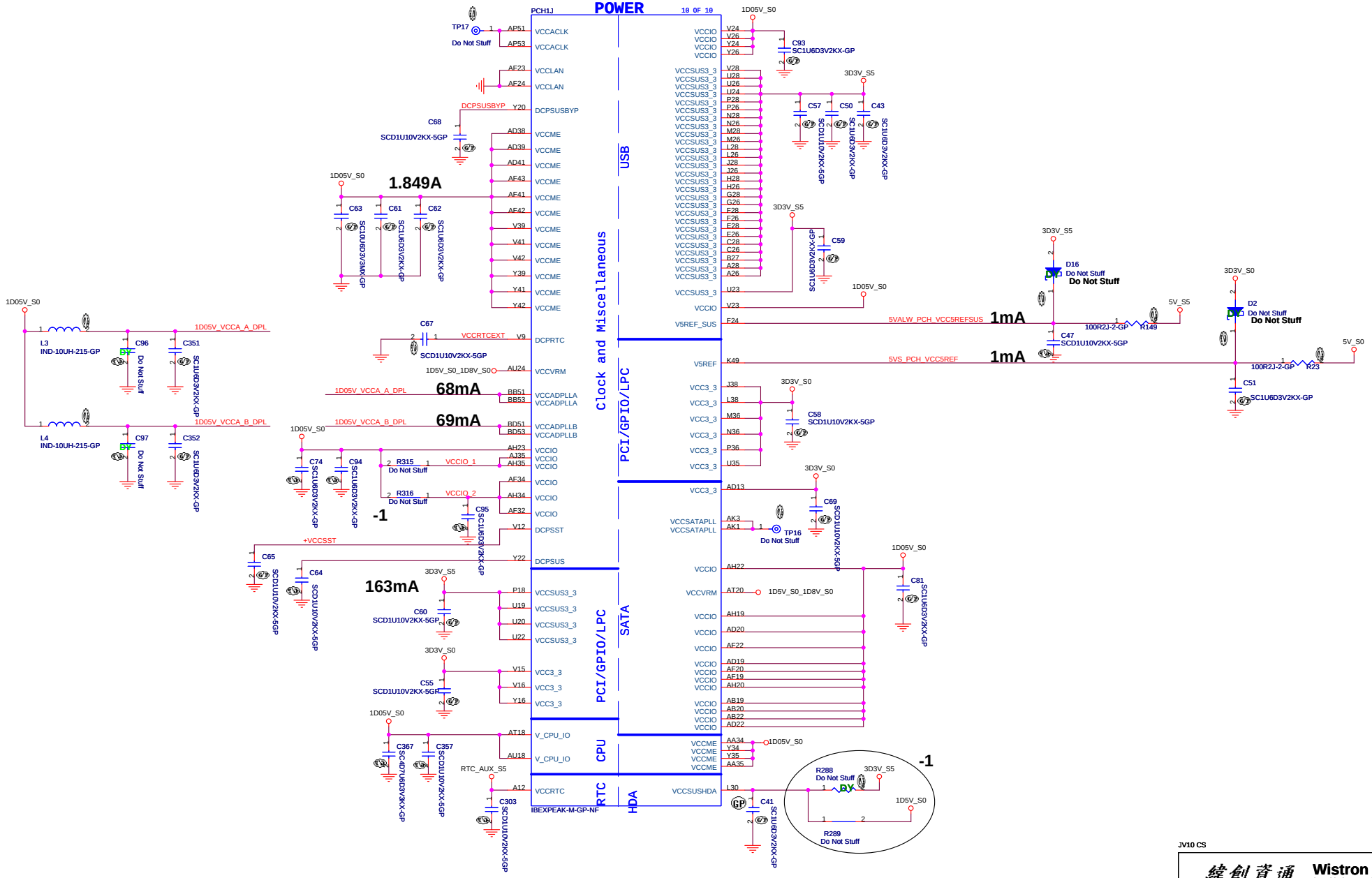
JV10 CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 7 of 9(PWR/VCORE/LVDS)

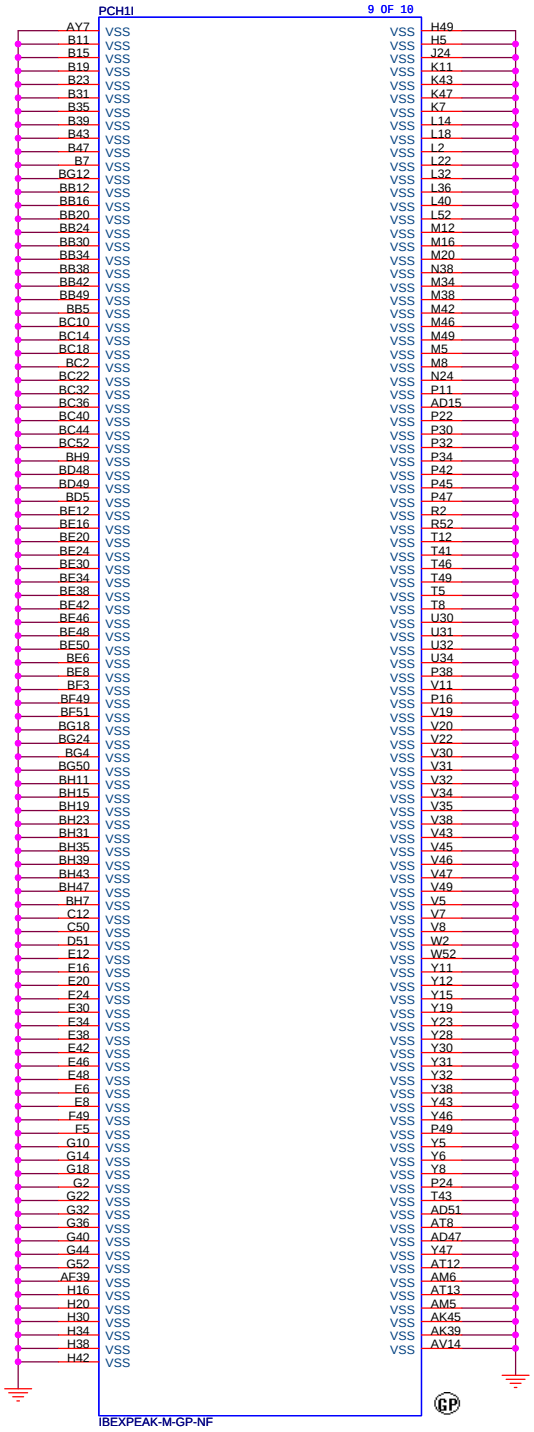
Size: Custom | Document Number: JV10-CS | Rev: -1

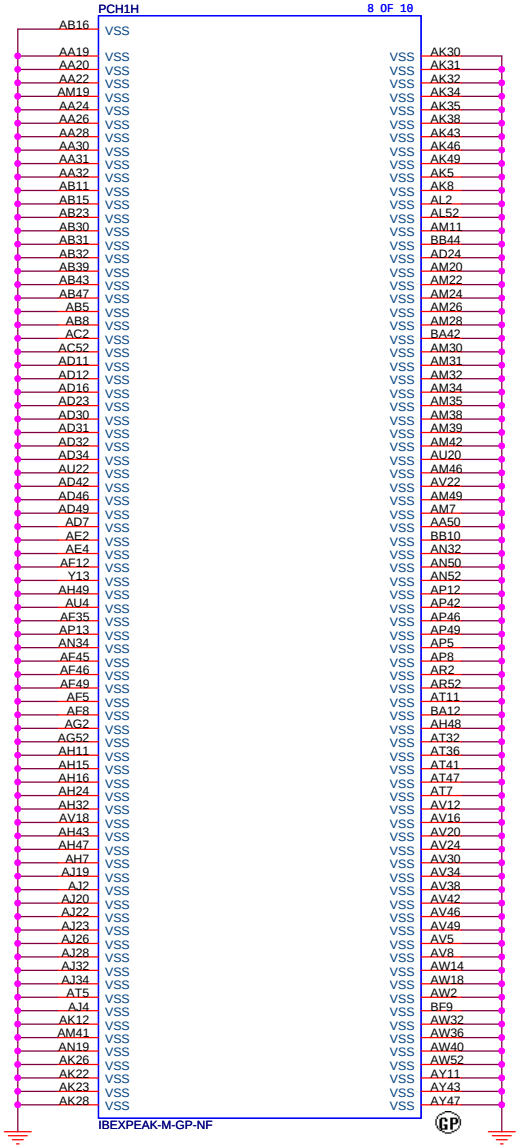
Date: Friday, January 22, 2010 | Sheet 18 of 50



JV10 CS

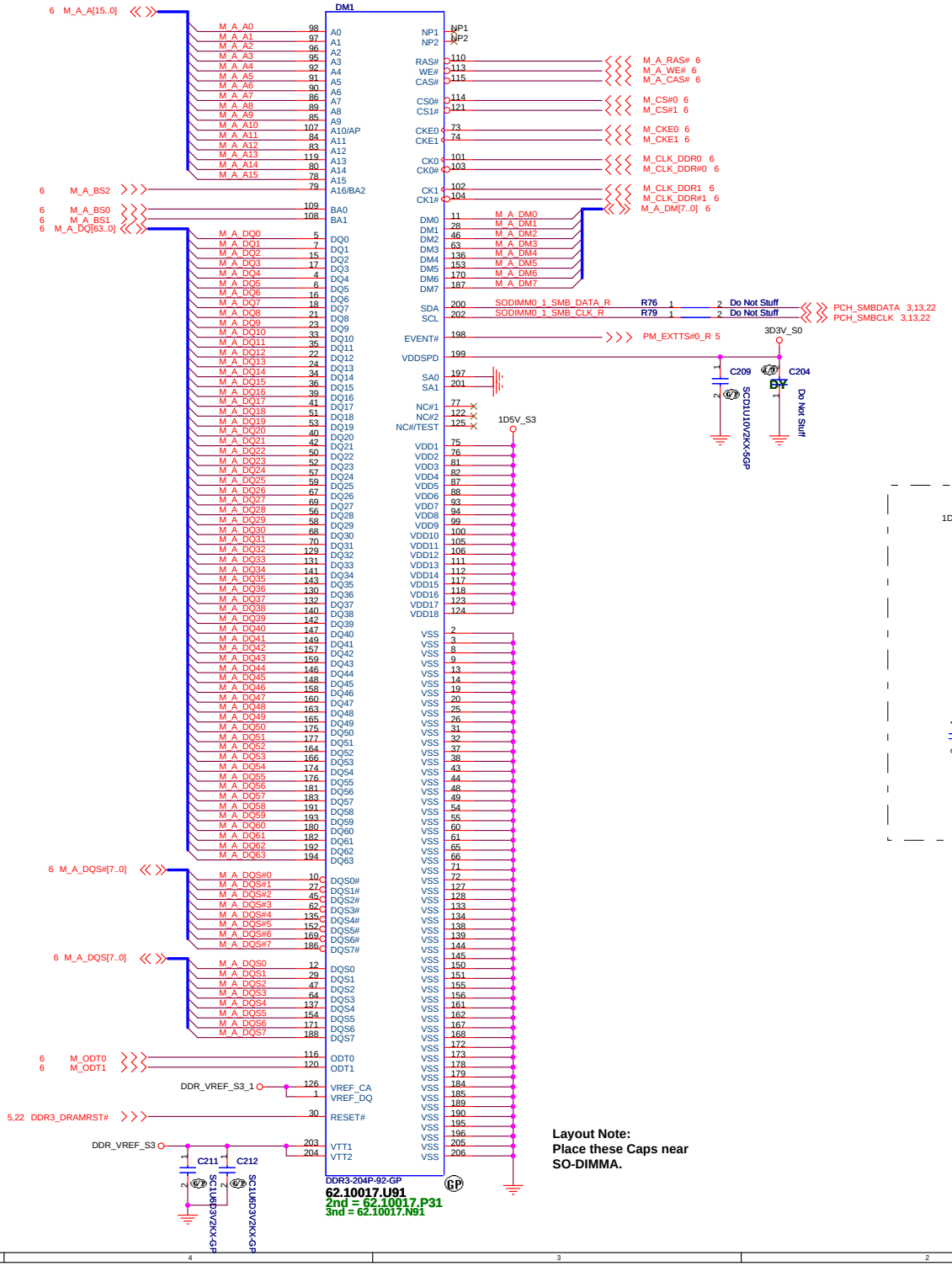
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH 8 of 9(PWR\SATA\USB)	
Size Custom	Document Number JV10-CS	Rev -1
Date: Friday, January 22, 2010	Sheet 19 of 50	



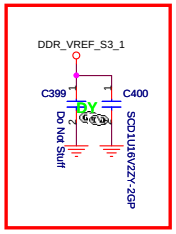


JV10 CS

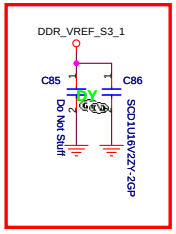
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**PCH 9 of 9(VSS)**	
Size A3	Document Number **JV10-CS**	Rev **-1**
Date: Friday, January 22, 2010	Sheet 20 of 50	



Layout Note：Near Pin 126

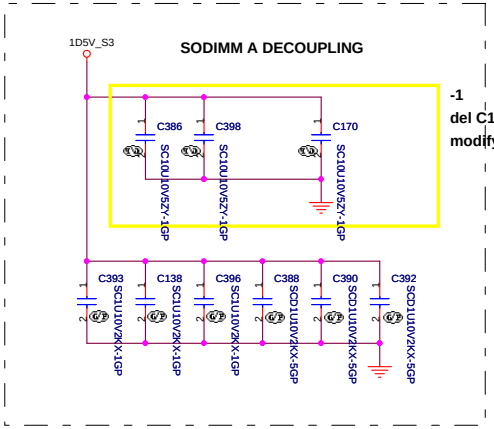


Layout Note：Near Pin 1



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



-1
del C129 C183
modify C386,C398,C170

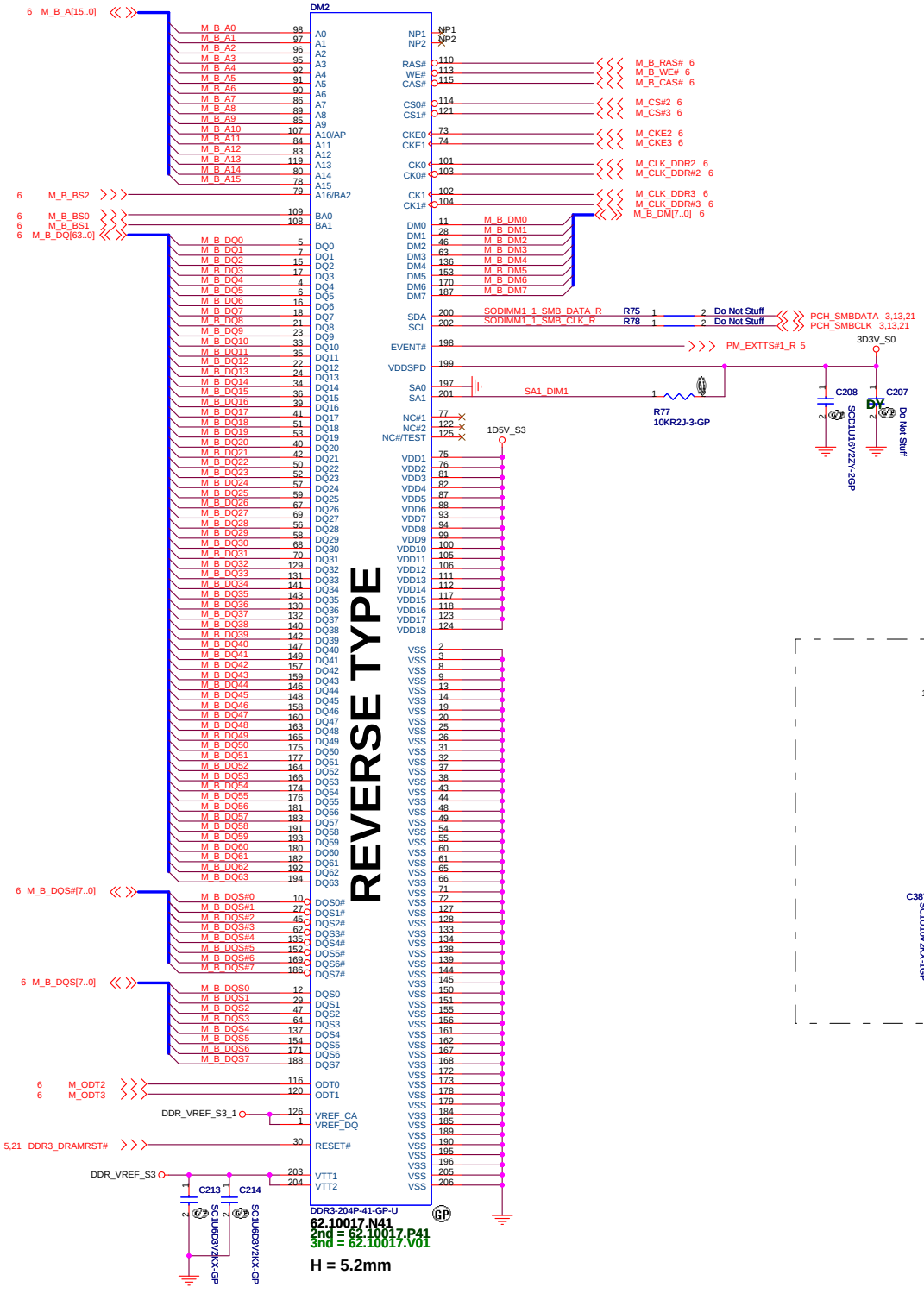
JV10 CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

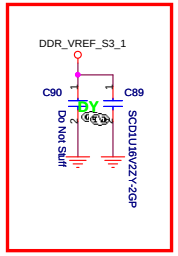
Title: **DDR3 SODIMM1**

Size	Document Number	Rev
Custom	JV10-CS	-1

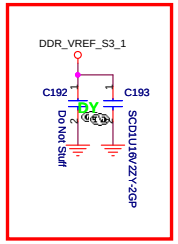
Date: Friday, January 22, 2010 Sheet 21 of 50

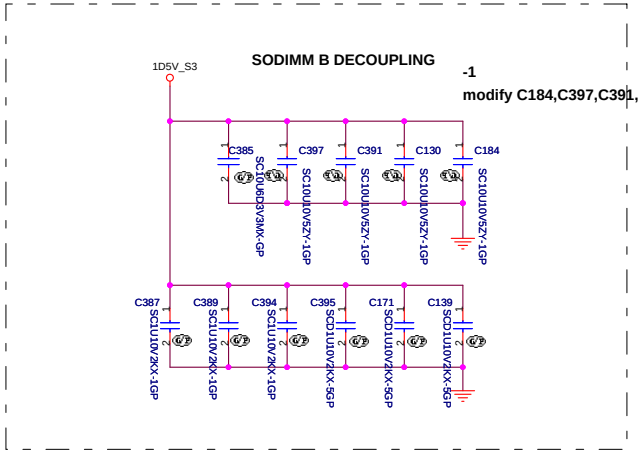


Layout Note：Near Pin 1



Layout Note：Near Pin 126





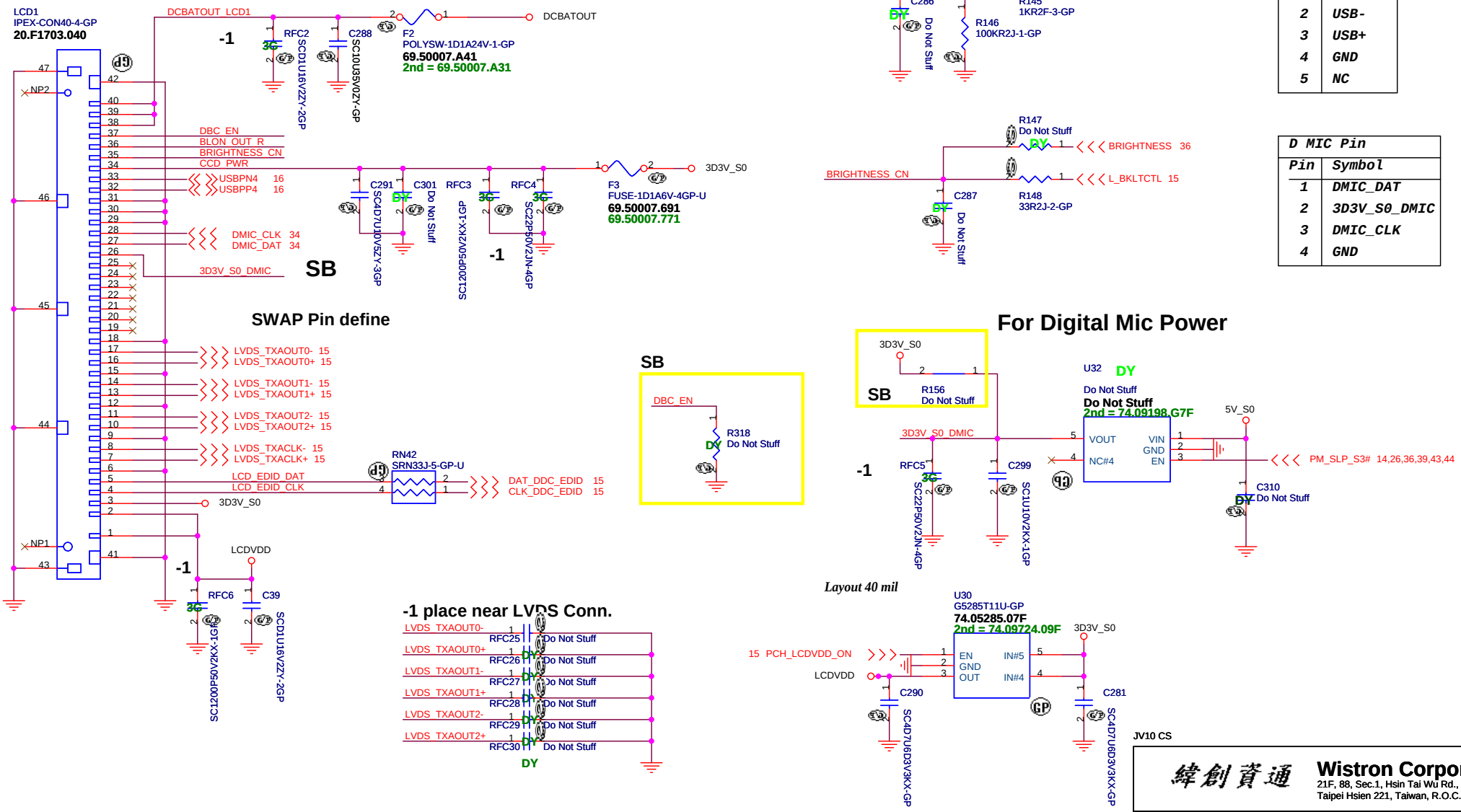
JV10 CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR3 SODIMM2**

Size	Document Number	Rev
Custom	JV10-CS	-1

Date: Friday, January 22, 2010 Sheet 22 of 50



CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	NC

D MIC Pin	
Pin	Symbol
1	DMIC_DAT
2	3D3V_S0_DMIC
3	DMIC_CLK
4	GND

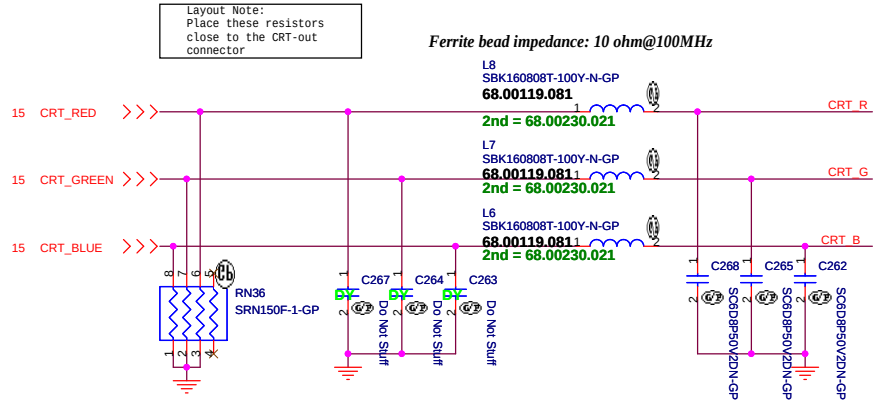
JV10 CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CCD CONN**

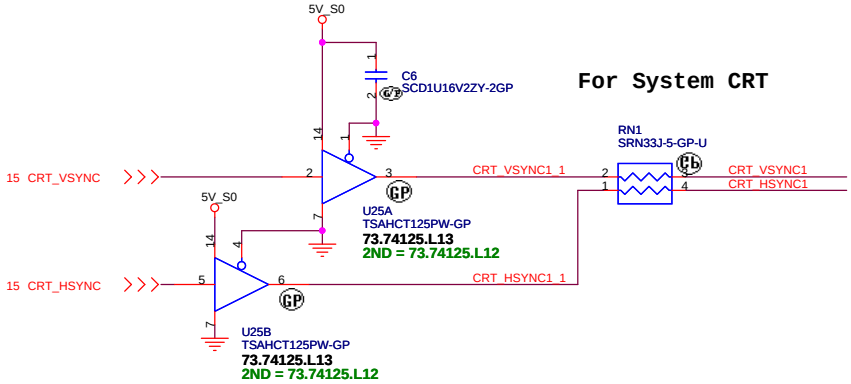
Size: Custom | Document Number: **JV10-CS** | Rev: **-1**

Date: Friday, January 22, 2010 | Sheet 23 of 50

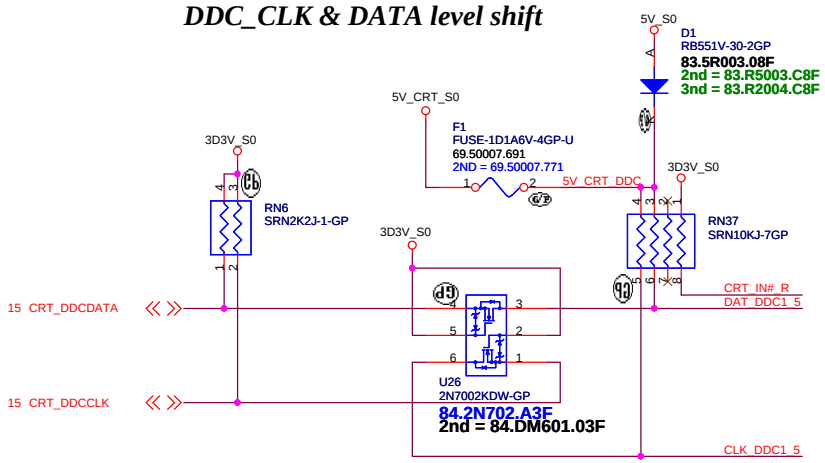


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

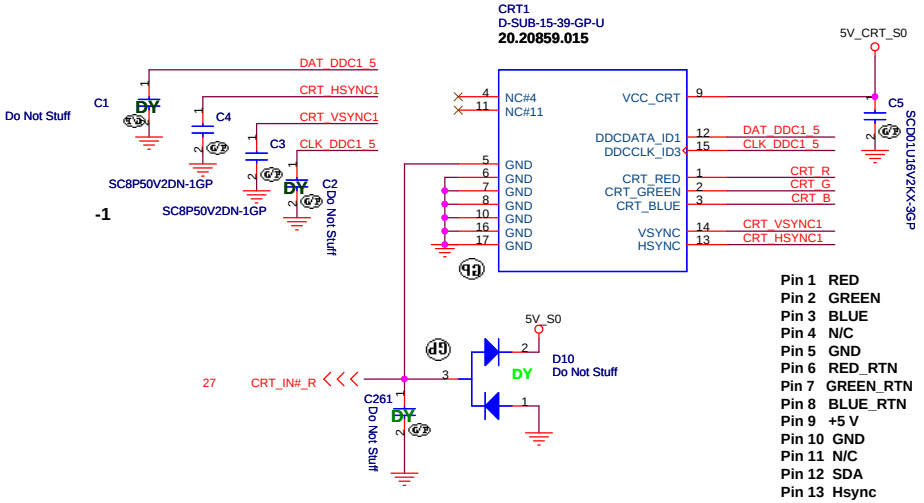
Hsync & Vsync level shift



DDC_CLK & DATA level shift



CRT I/F & CONNECTOR



Pin 1 RED
Pin 2 GREEN
Pin 3 BLUE
Pin 4 N/C
Pin 5 GND
Pin 6 RED_RTN
Pin 7 GREEN_RTN
Pin 8 BLUE_RTN
Pin 9 +5 V
Pin 10 GND
Pin 11 N/C
Pin 12 SDA
Pin 13 Hsync
Pin 14 VSync
Pin 15 SCL

JV10 CS

緯創資通 **Wistron Corporation**
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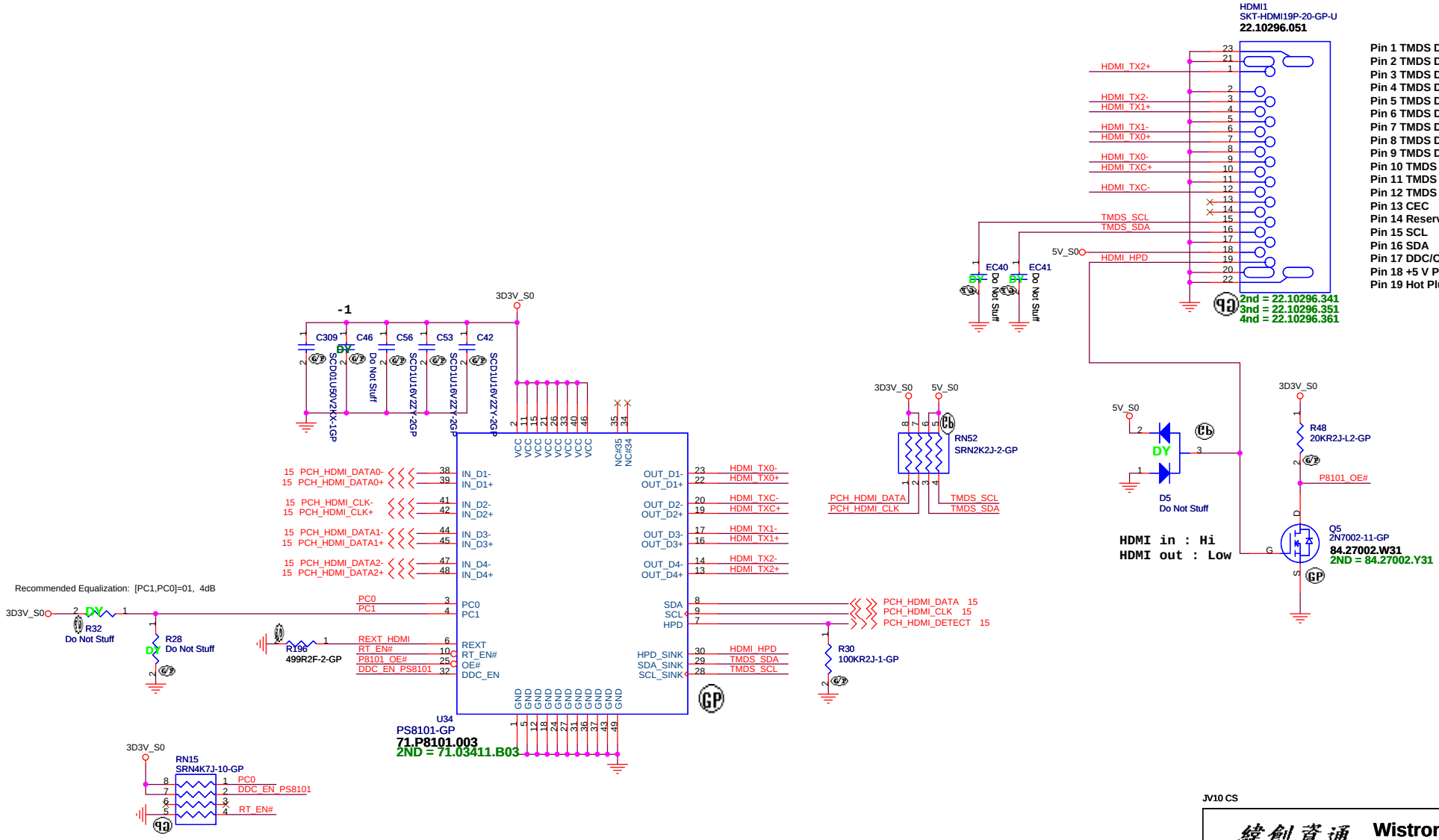
Taipei Hsien 221, Taiwan, R.O.C.

Title	**CRT conn**	
Size A3	Document Number **JV10-CS**	Rev **-1**
Date: Friday, January 22, 2010	Sheet 24 of 50	

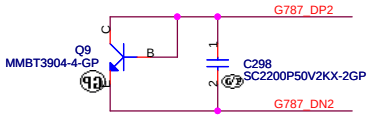
HDMI CONNECTOR



JV10 CS

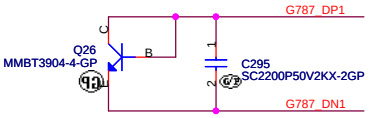
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**HDMI conn**	
Size Custom	Document Number **JV10-CS**	Rev **-1**
Date: Friday, January 22, 2010	Sheet 25 of 50	

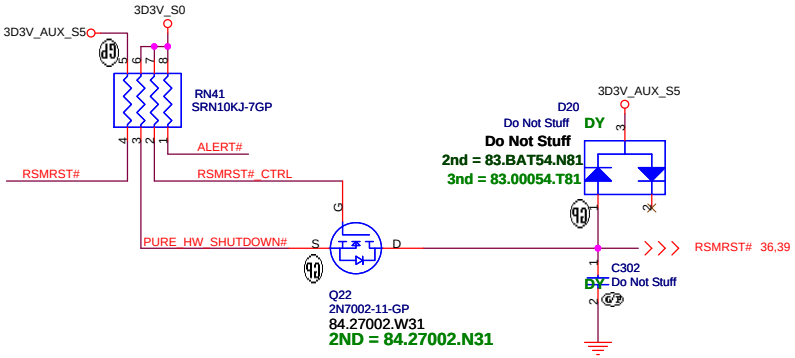
For T8 thermal diode



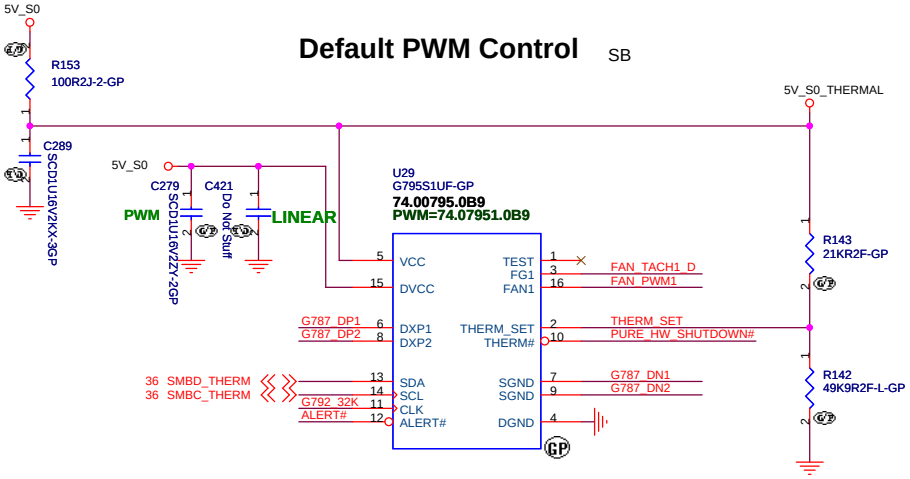
C298& C295 CLOSE to G795

For System thermal diode

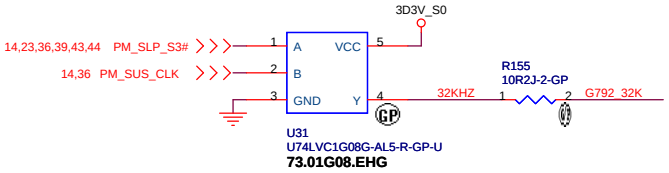




Default PWM Control SB



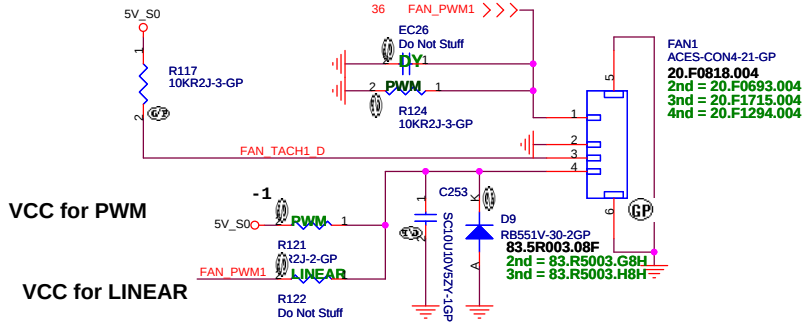
T8=90C
THERM_SET = [(Tset-72) x 0.02+0.34] x VCC



CPU FAN Connector

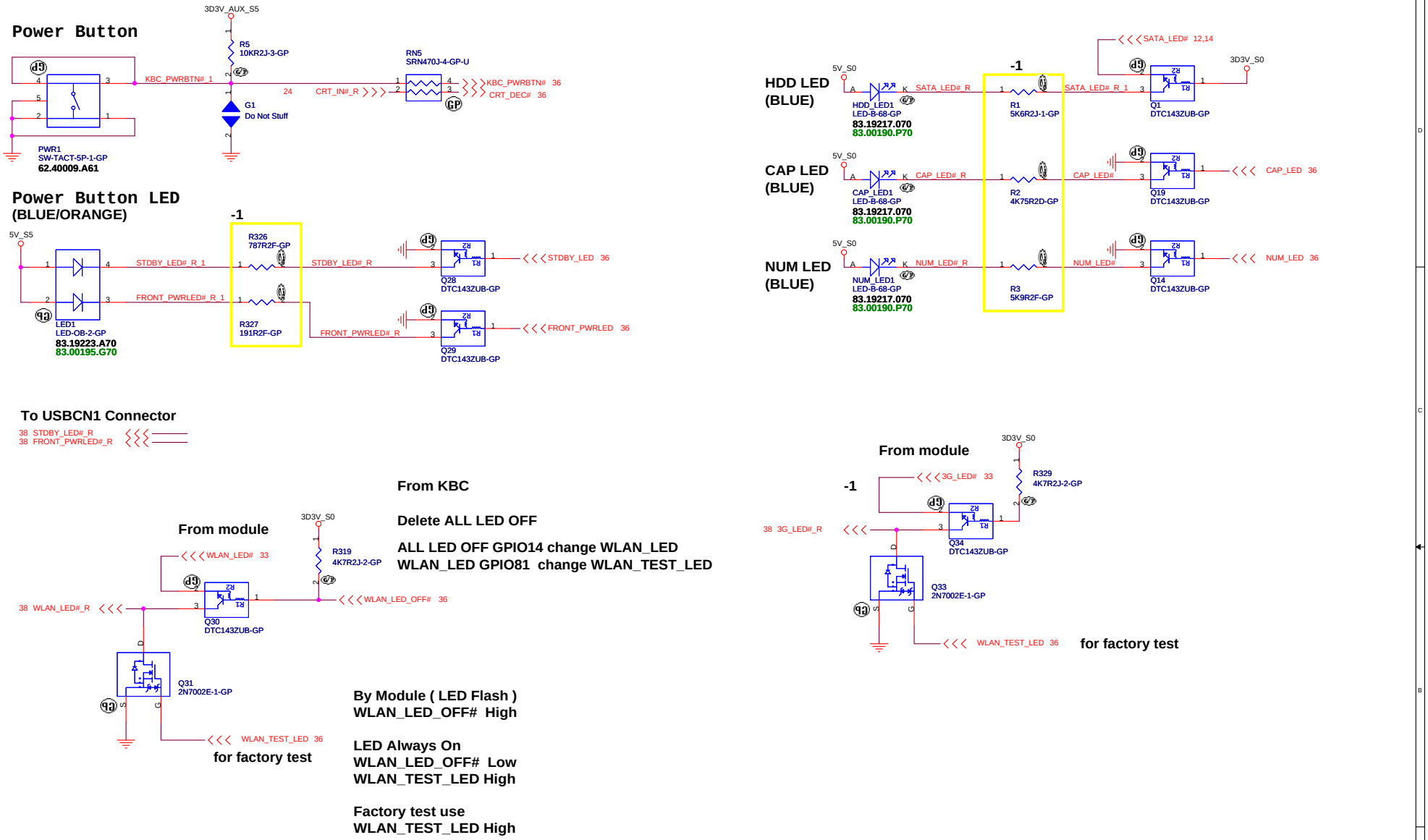
PWM FAN		LINEAR FAN	
PIN1	PWM	PIN1	NC
PIN2	GND	PIN2	GND
PIN3	FG	PIN3	FG
PIN4	VCC	PIN4	VCC

PWM FOR EC



JV10 CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Thermal/Fan Conn
Size A3 / Document Number	JV10-CS
Rev	-1
Date: Friday, January 22, 2010	Sheet 26 of 50

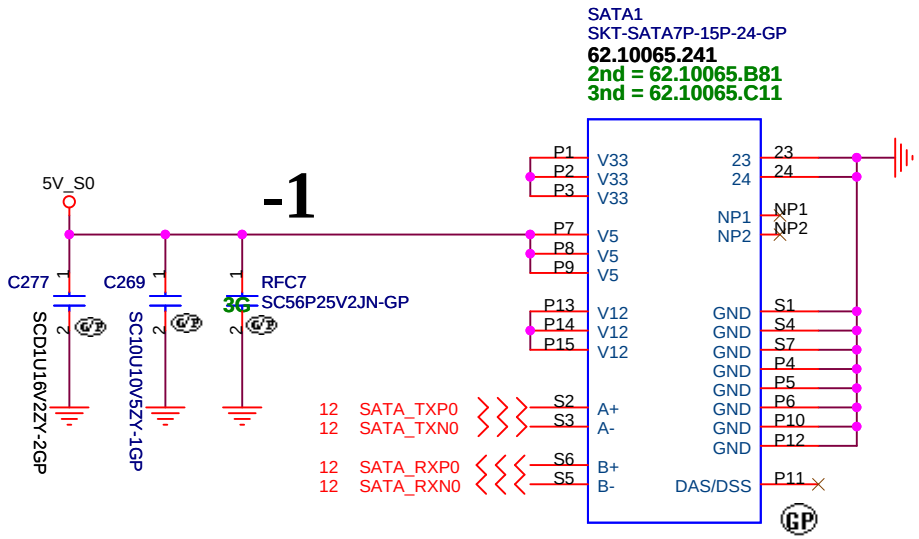


JV10 CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED	
Size: Custom	Document Number: JV10-CS	Rev: -1
Date: Friday, January 22, 2010	Sheet 27 of 50	

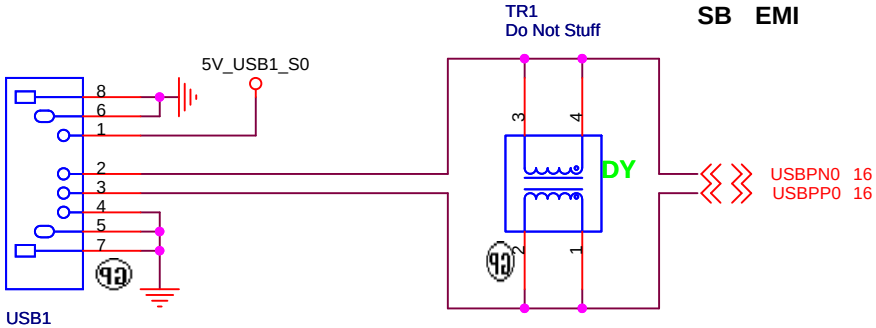
SATA Connector

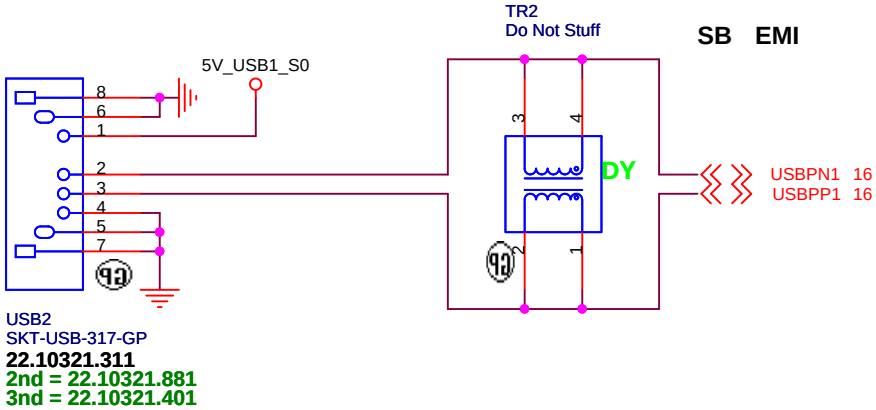


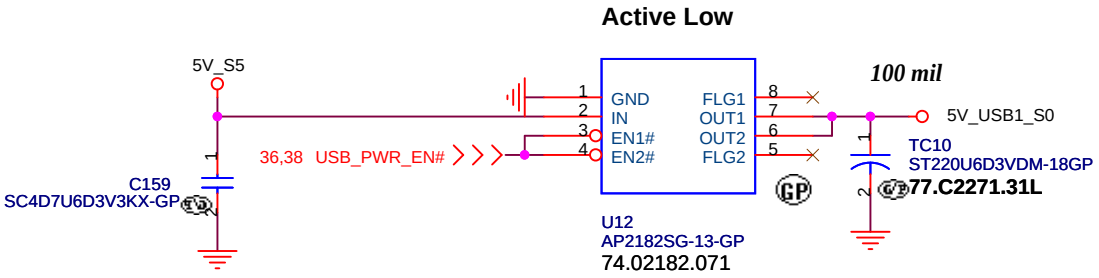
JV10 CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***HDD***		
Size A4	Document Number	JV10-CS	Rev *-1*
Date: Friday, January 22, 2010	Sheet 28 of 50		

USB MODULE





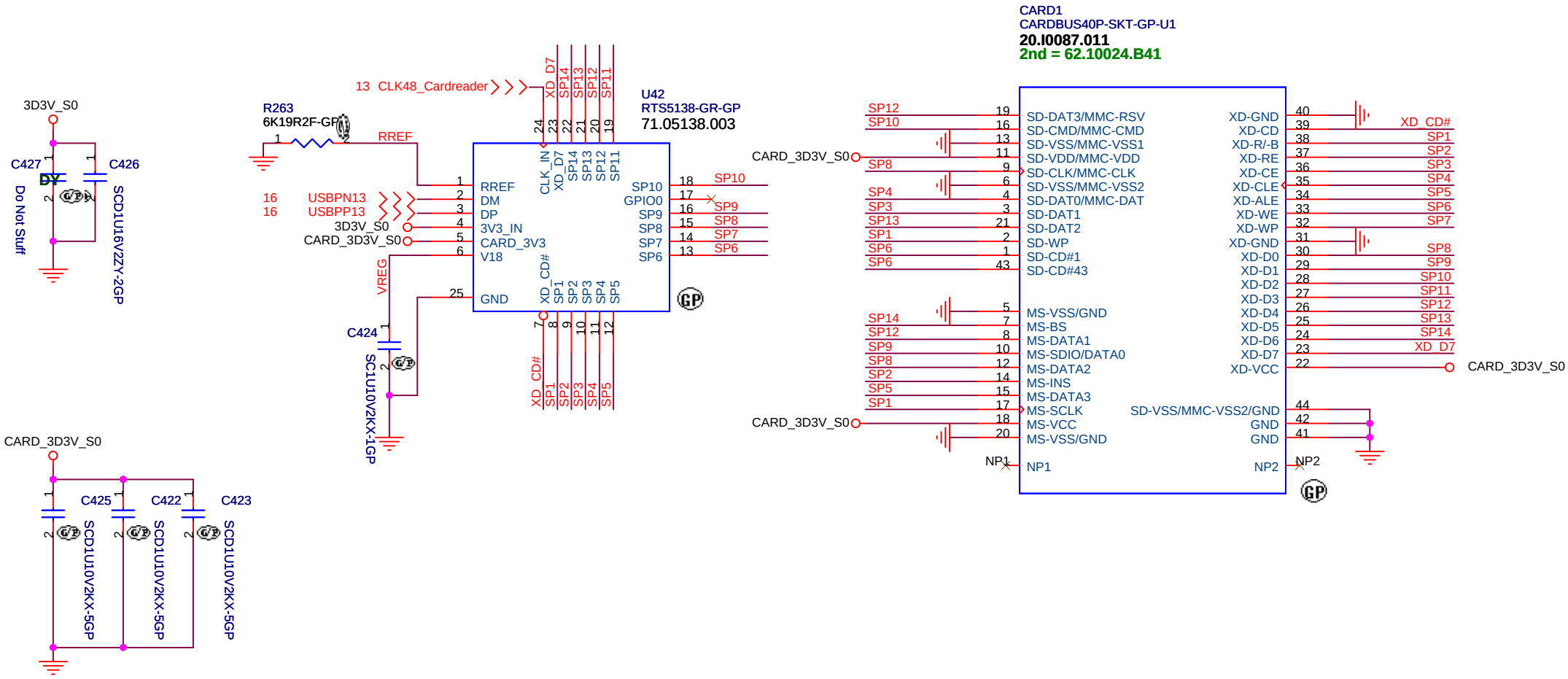


JV10 CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB Port***	
Size A4	Document Number JV10-CS	Rev -1
Date: Friday, January 22, 2010	Sheet 29 of 50	

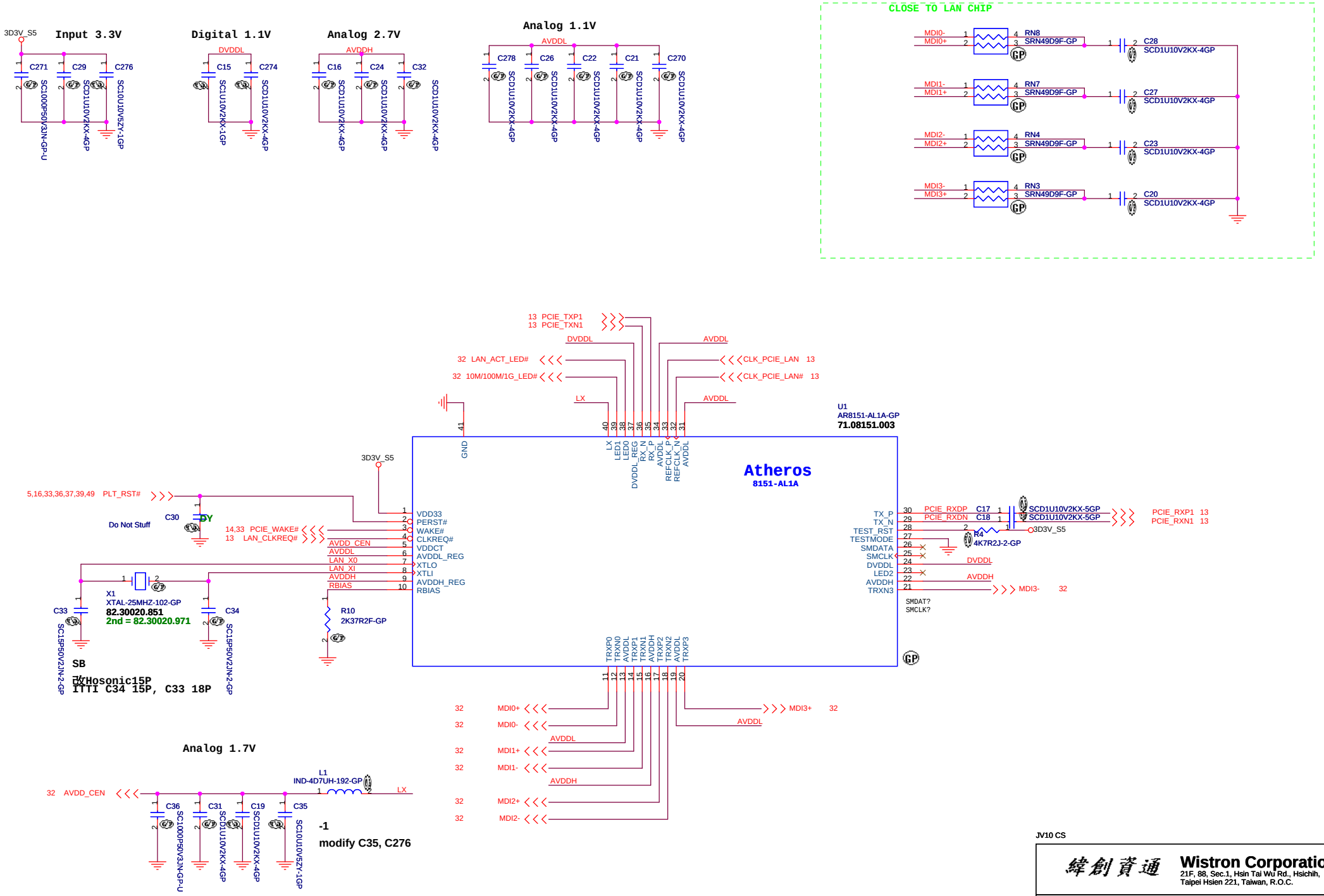
5 IN1 CARD-READER

SB
與 ALPS Co-Layout



JV10 CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	CARDREADER		
Size A4	Document Number JV10-CS		Rev -1
Date: Friday, January 22, 2010	Sheet 30 of 50		



JV10 CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AR8151 chip**

Size: A3 | Document Number: **JV10-CS** | Rev: **-1**

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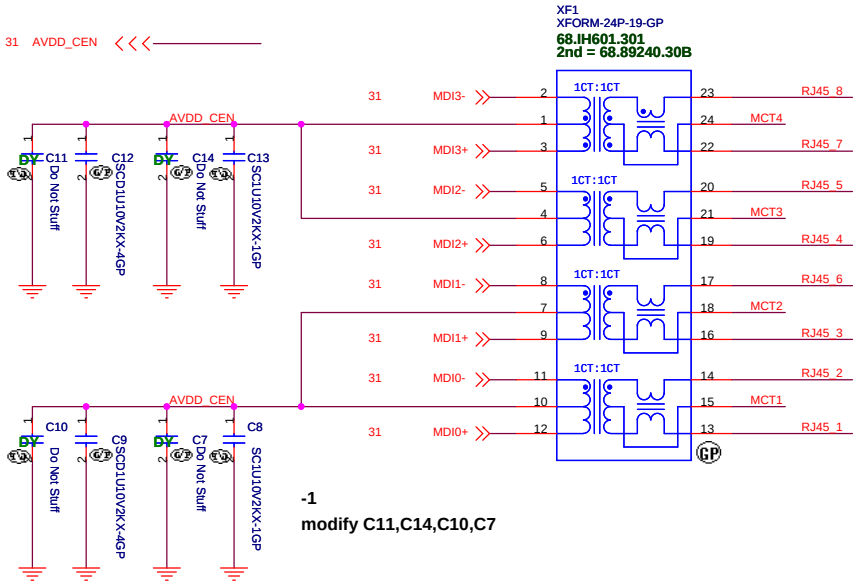
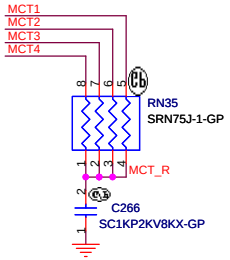
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

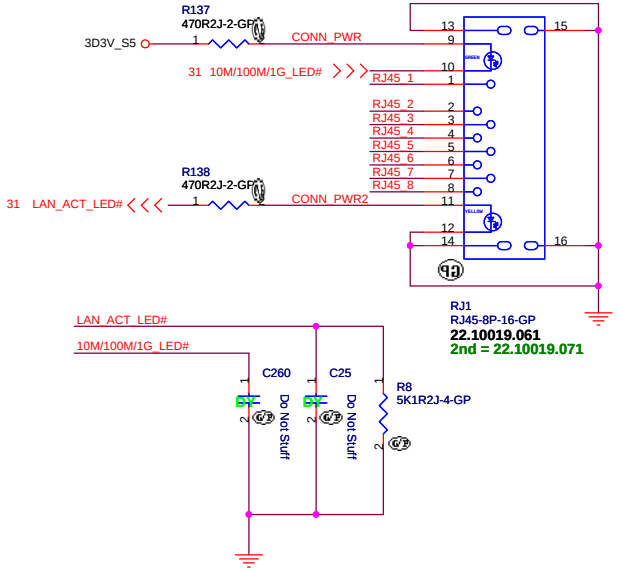
LAN Connector

GIGA Lan Transformer



-1
modify C11,C14,C10,C7





LED COLOR

B1(+) B2(-)::GREEN

A1(+) A2(-):YELLOW

Green(A3), behavior is the same for 10/100/1000 bits

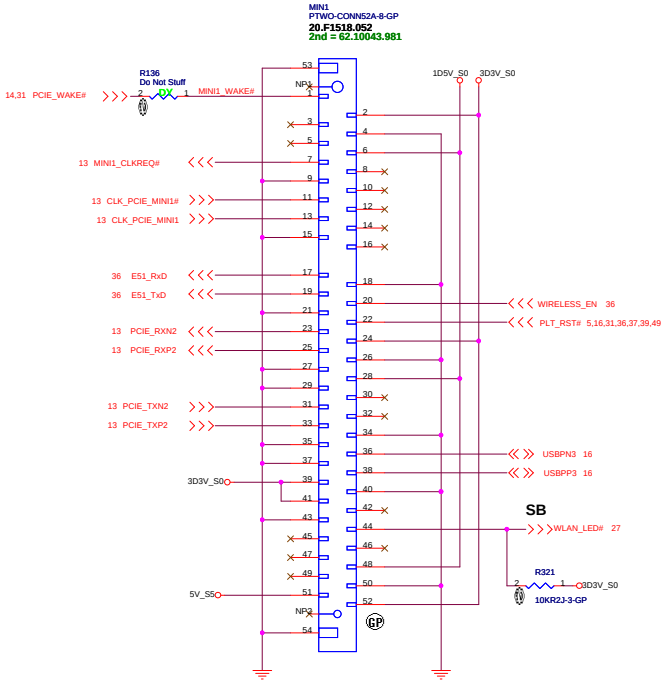
Yellow(B2), when LAN is transfering data.

JV10 CS

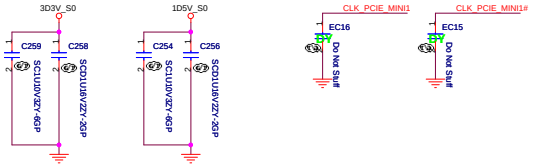
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN Connector	
Size A3	Document Number JV10-CS	Rev -1
Date: Friday, January 22, 2010	Sheet 32 of 50	

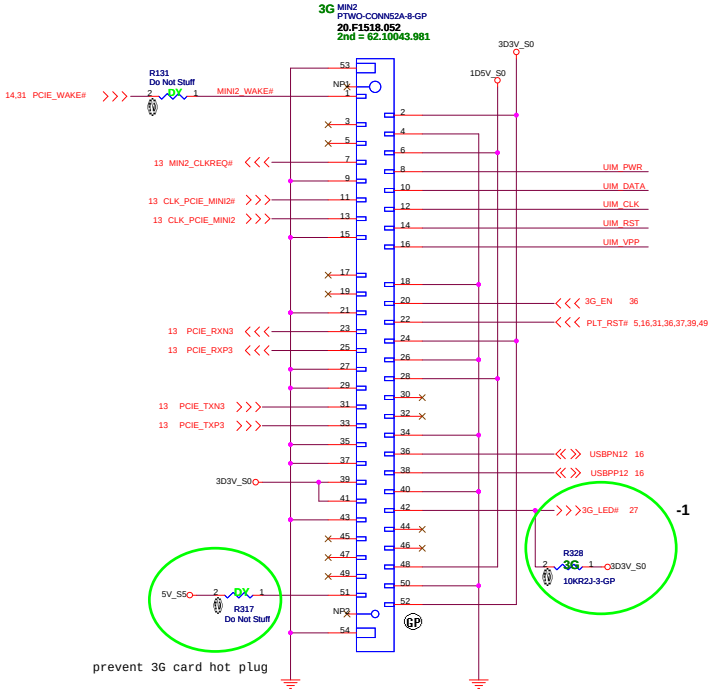
Mini Card Connector(WLAN)
Support debug-card



Place near MINI1

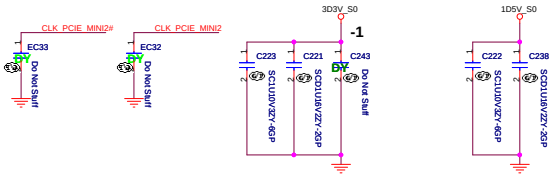


Mini Card Connector(3G)

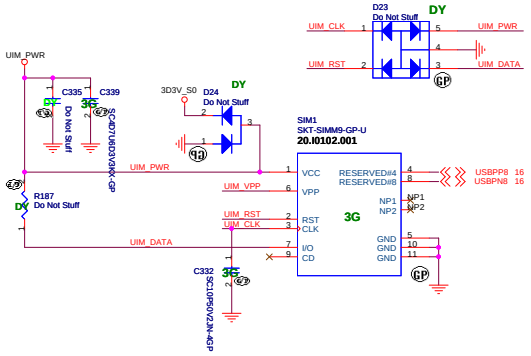


prevent 3G card hot plug

Place near MINIC2

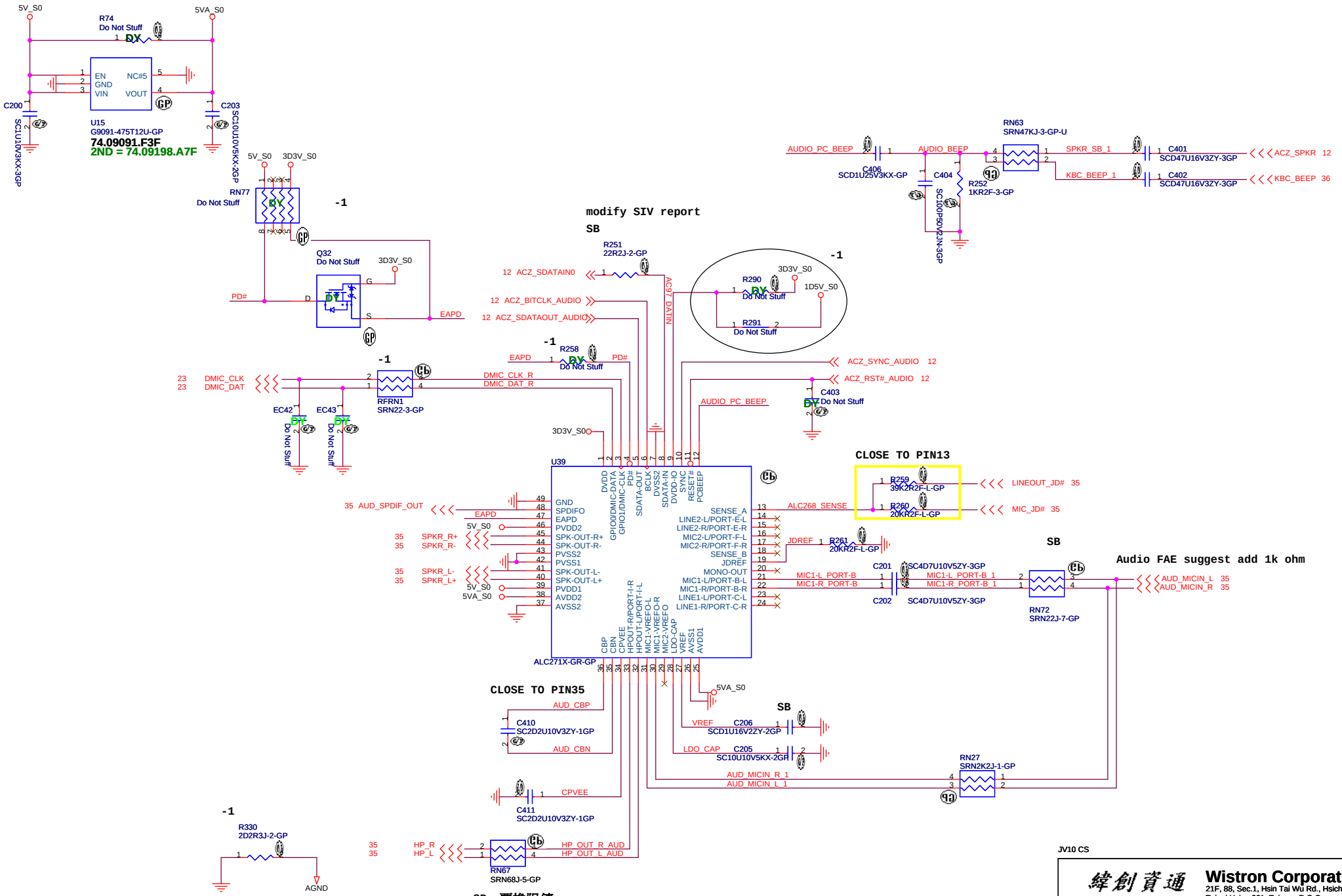


SIM Card



JV10 CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINI Conn	
Size Custom	Document Number JV10-CS	Rev -1
Date: Friday, January 22, 2010	Sheet 33 of 50	

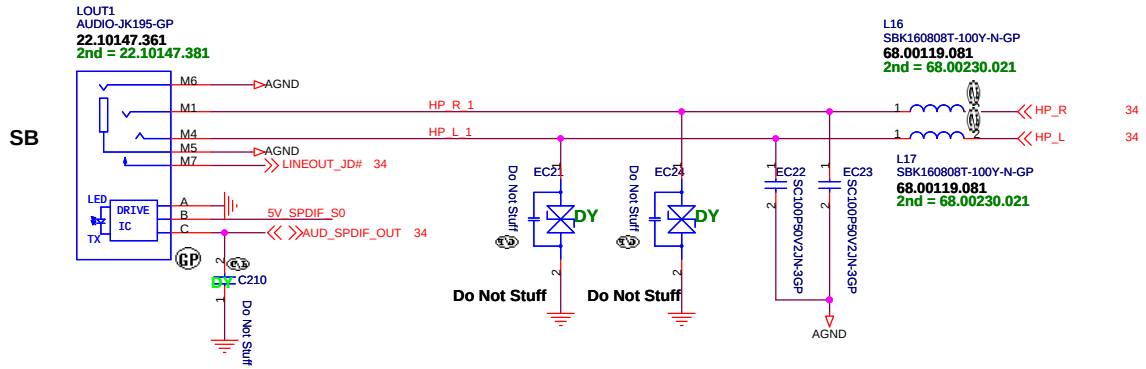


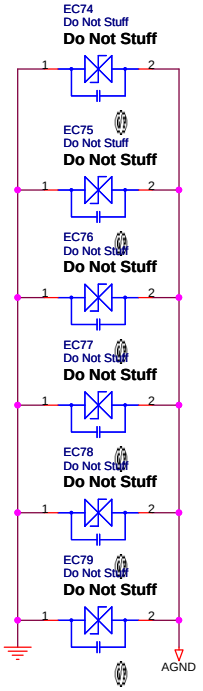
JV10 CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

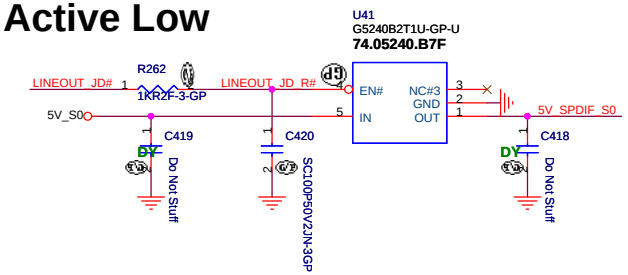
Title	**Audio ALC271X**		
Size Custom	Document Number **JV10-CS**		Rev **-1**
Date: Friday, January 22, 2010	Sheet 34 of 50		

LINE OUT

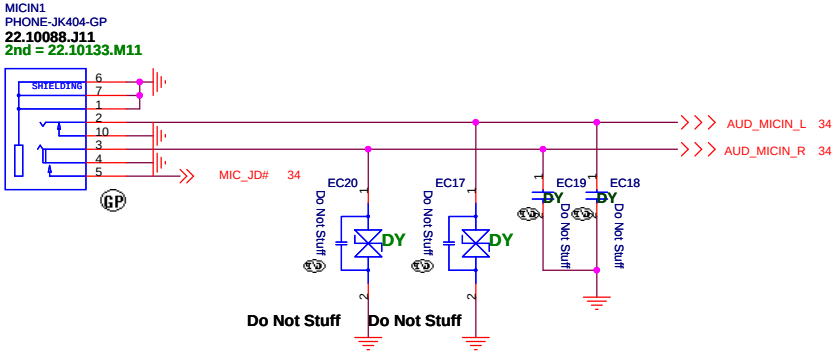




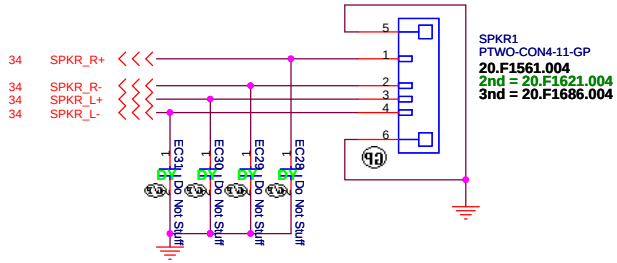
Active Low



MIC IN

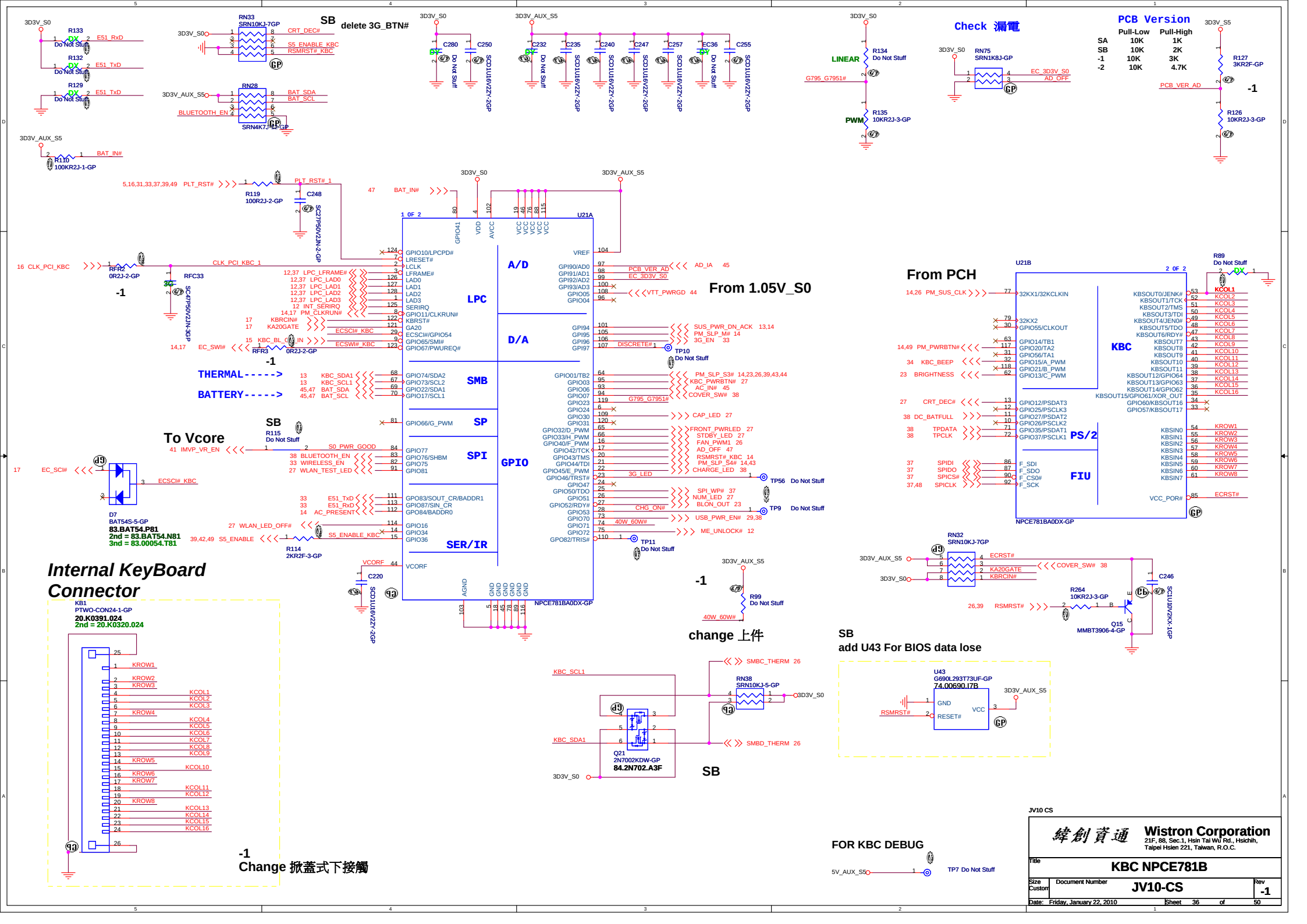


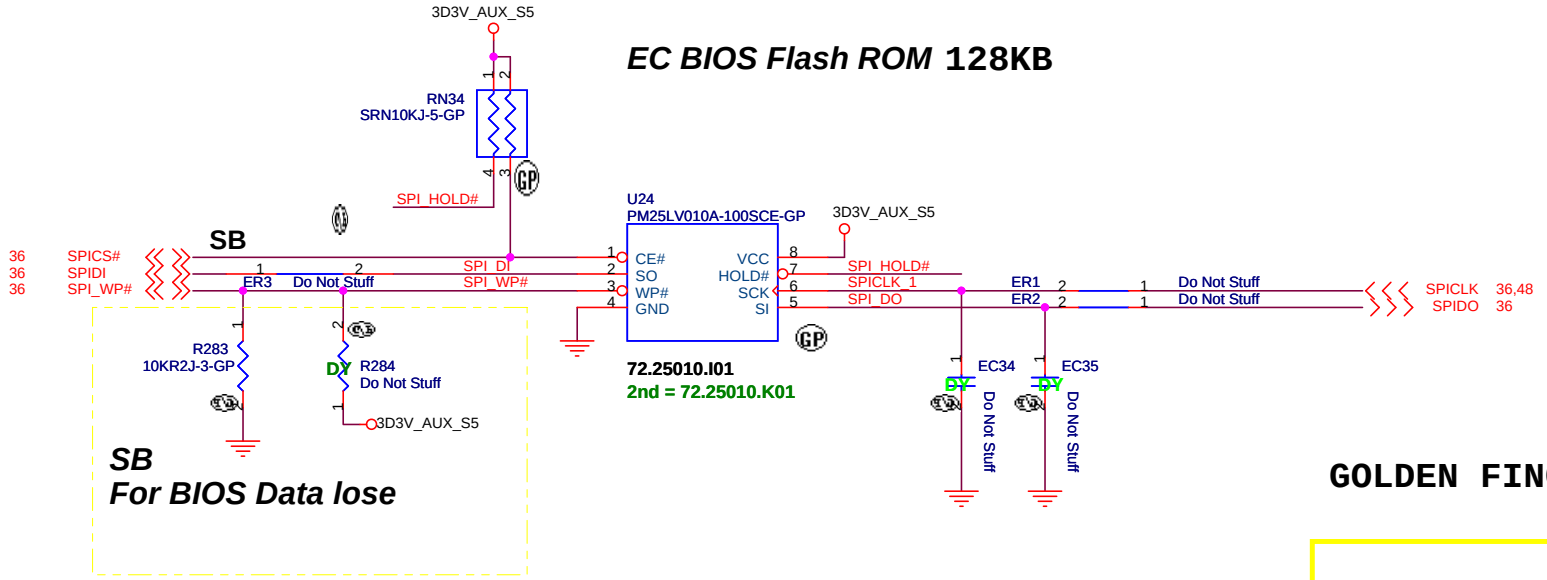
Internal Speaker



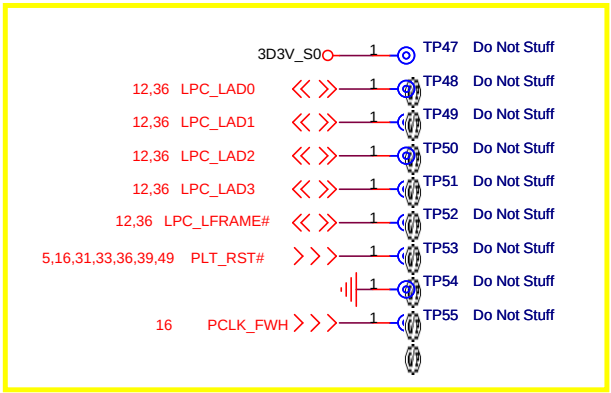
JV10 CS

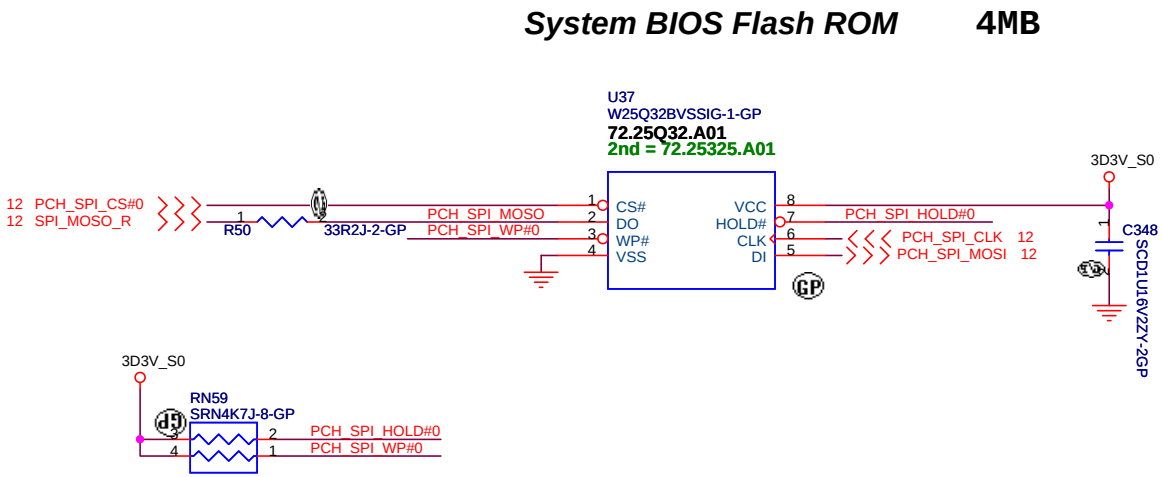
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Audio Jack/Mic In/ SPKR***	
Size A3	Document Number JV10-CS	Rev -1
Date: Friday, January 22, 2010	Sheet 35 of 50	


SB delete 3G_BTN#
Check 漏電
PCB Version
Pull-Low Pull-High
SA 10K 1K
SB 10K 2K
-1 10K 3K
-2 10K 4.7K
From 1.05V_S0
From PCH
To Vcore
THERMAL----->
BATTERY----->
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
U21A
U21B
KBC
PS/2
FIU
NPCE781BA0DX-GP
Internal KeyBoard Connector
KB1
PTWO-CON24-1-GP
20.K0391.024
2nd = 20.K0320.024
-1
Change 掀蓋式下接觸
change 上件
SB
add U43 For BIOS data lose
U43
G690L293T73UF-GP
74.00690.I7B
Q21
2N7002KDW-GP
84.2N702.A3F
FOR KBC DEBUG
TP7 Do Not Stuff
JV10 CS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC NPCE781B
Size Custom
Document Number
JV10-CS
Rev -1
Date: Friday, January 22, 2010
Sheet 36 of 50



GOLDEN FINGER FOR DEBUG BOARD



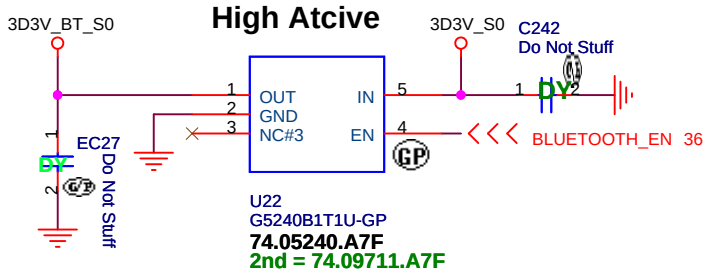


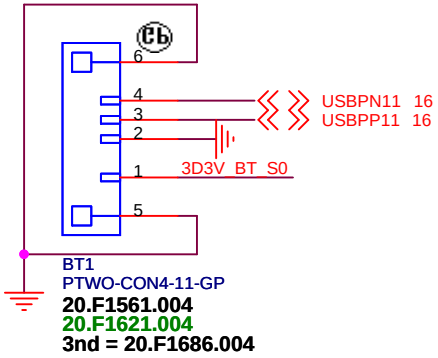
JV10 CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

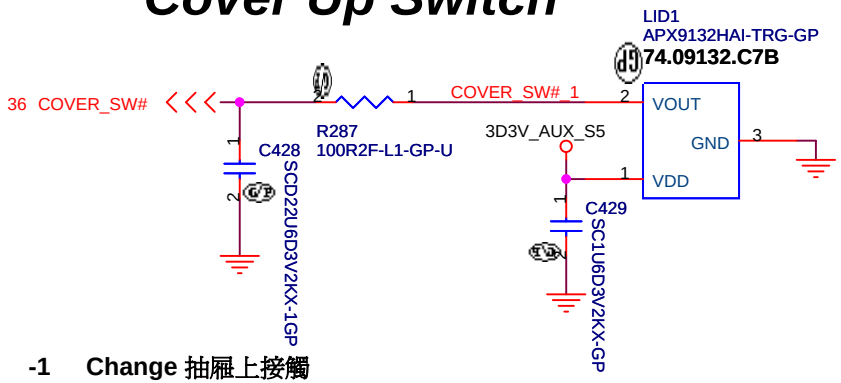
Title	BIOS		
Size Custom	Document Number JV10-CS		Rev -1
Date: Friday, January 22, 2010	Sheet 37 of 50		

BLUETOOTH Connector



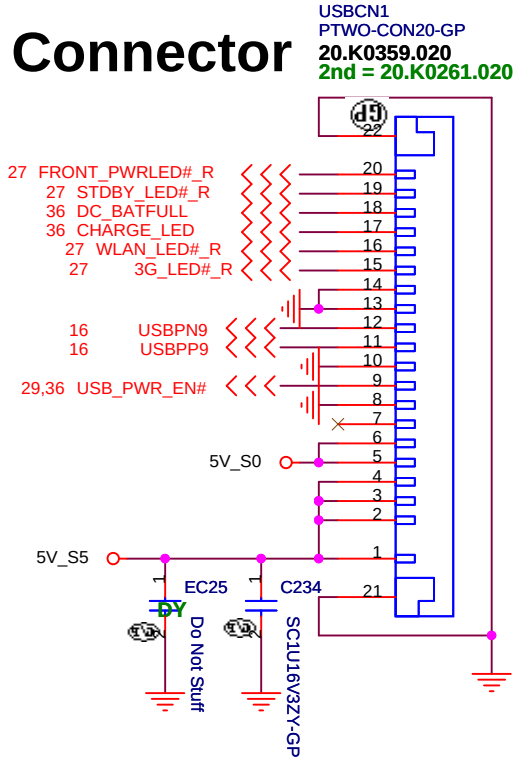


Cover Up Switch



-1 Change 抽屜上接觸

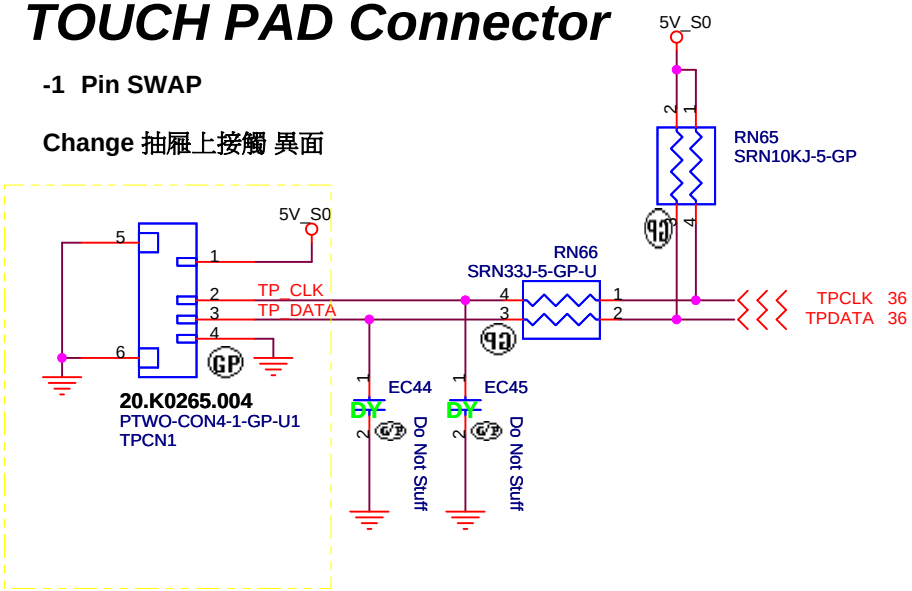
USB Connector



TOUCH PAD Connector

-1 Pin SWAP

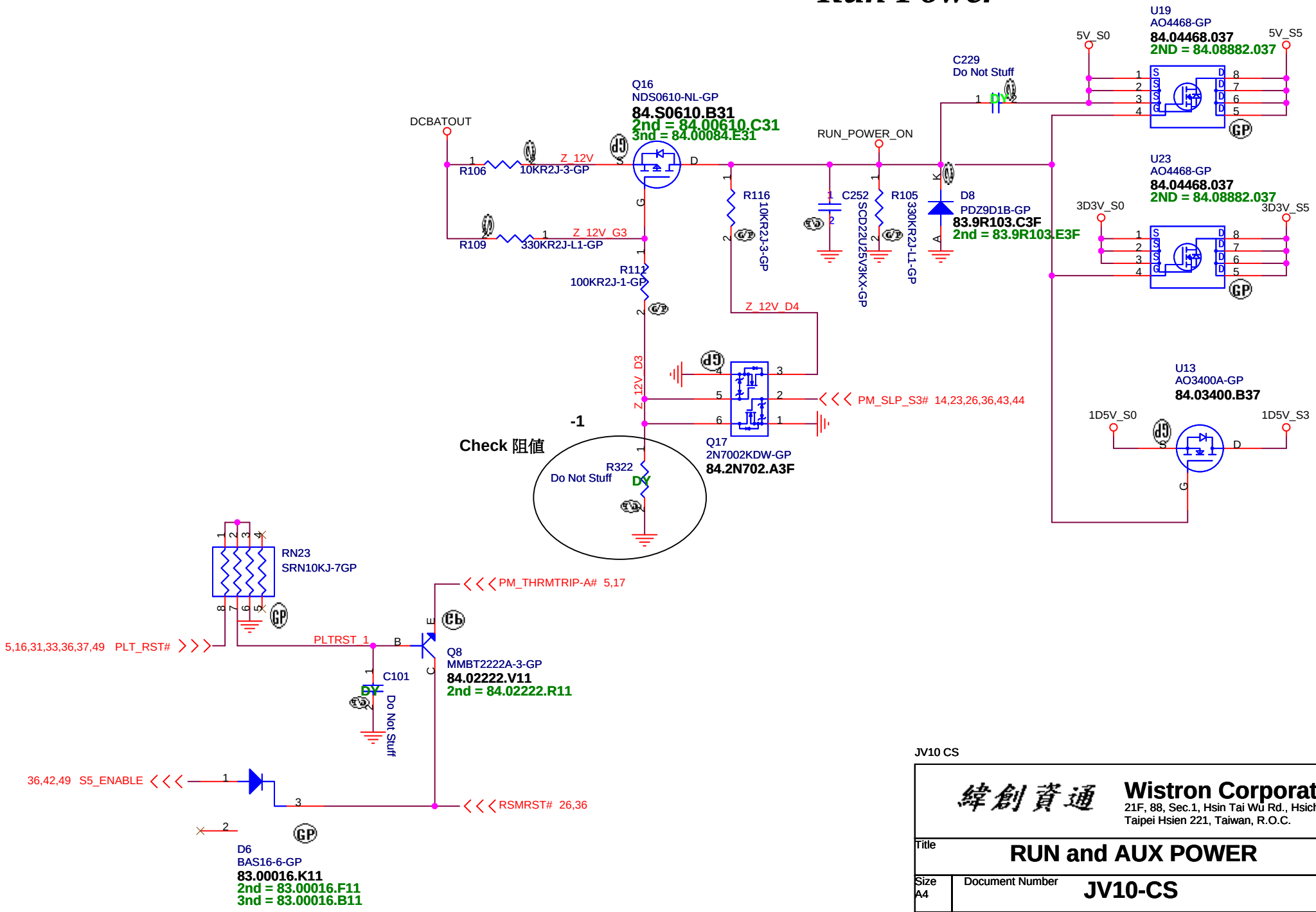
Change 抽屜上接觸 異面



JV10 CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	**CONNECTOR**		
Size A4	Document Number **JV10-CS**		Rev **-1**
Date: Friday, January 22, 2010		Sheet 38 of 50	

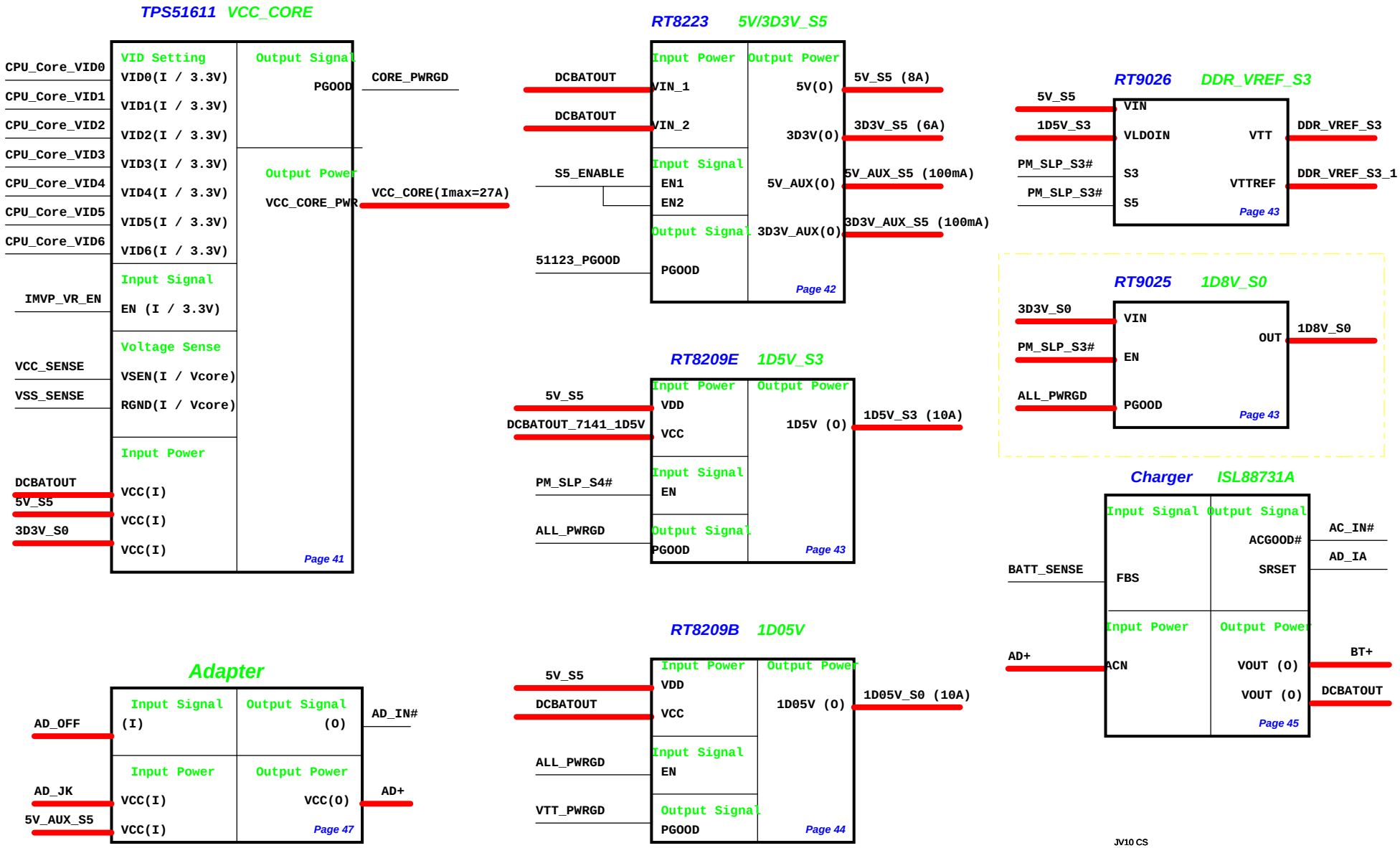
Run Power



JV10 CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN and AUX POWER	
Size A4	Document Number JV10-CS	Rev -1
Date: Friday, January 22, 2010	Sheet 39 of 50	



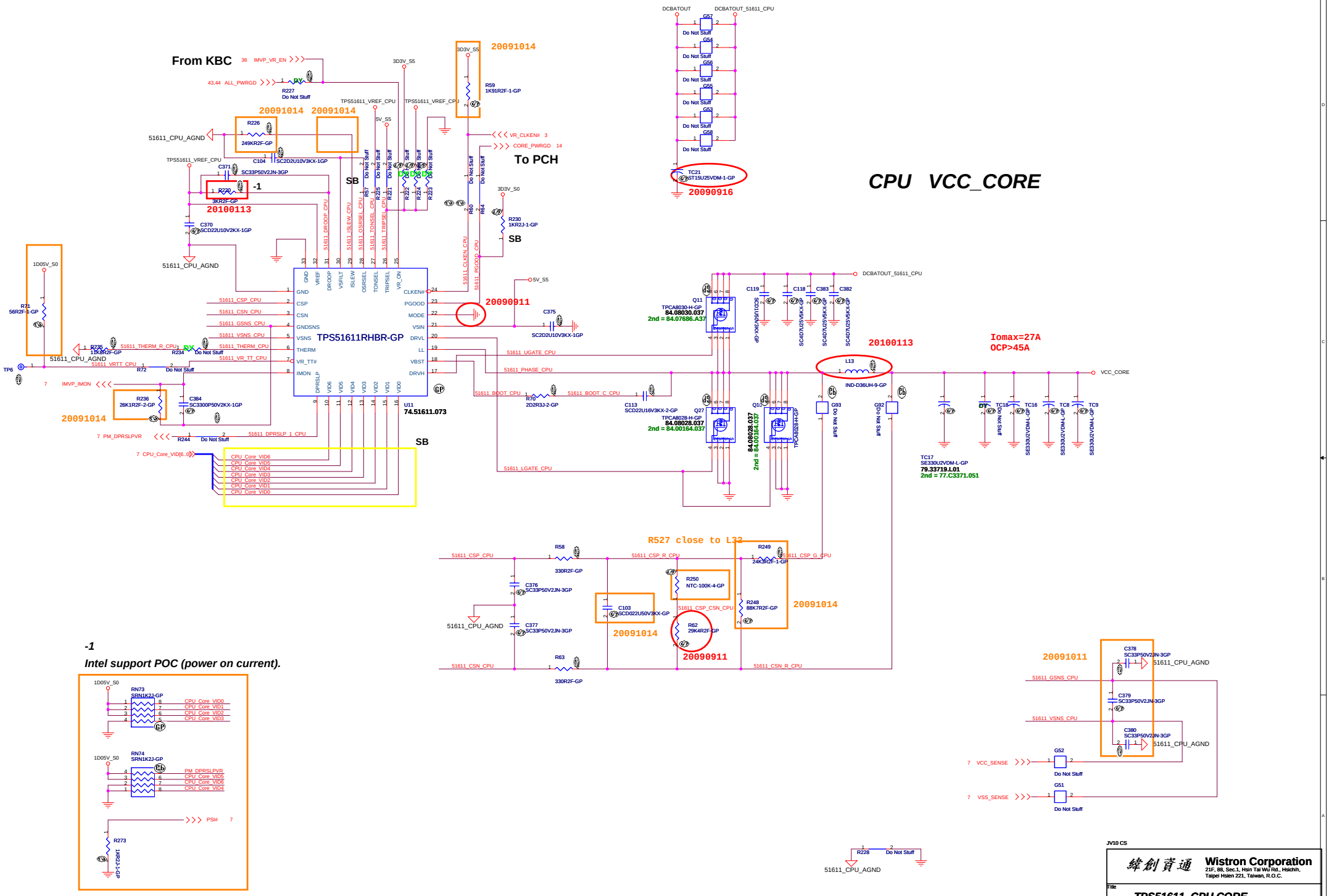
JV10 CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size | Document Number: JV10-CS | Rev: -1

Date: Friday, January 22, 2010 | Sheet 40 of 50


CPU VCC_CORE
From KBC
To PCH
TPS51611RHBR-GP
U11
74.51611.073
20091014
20100113
20090916
20090911
Iomax=27A
OCP>45A
R527 close to L32
-1
SB
DX
Do Not Stuff
VCC_CORE
51611_CPU_AGND
DCBATOUT_51611_CPU
Intel support POC (power on current).
RN73
SRN1K2J-GP
RN74
SRN1K2J-GP
CPU_Core_VID0
CPU_Core_VID1
CPU_Core_VID2
CPU_Core_VID3
CPU_Core_VID4
CPU_Core_VID5
CPU_Core_VID6
PM_DPRSLPVR
PSI#
R273
1K0R2J-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
JV10 CS
TPS51611_CPU CORE
JV10-CS
Rev
-1
Date: Friday, January 22, 2010
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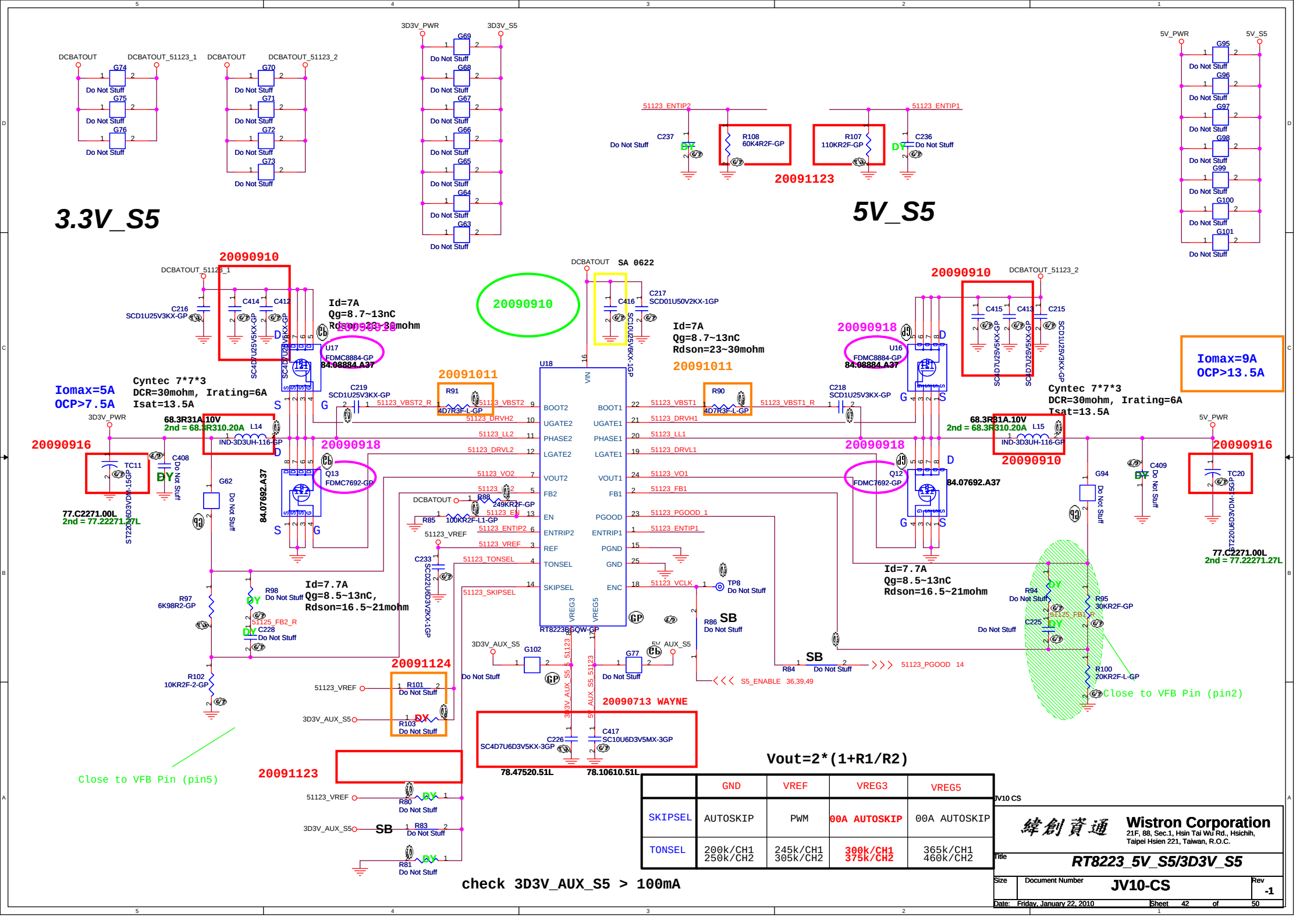
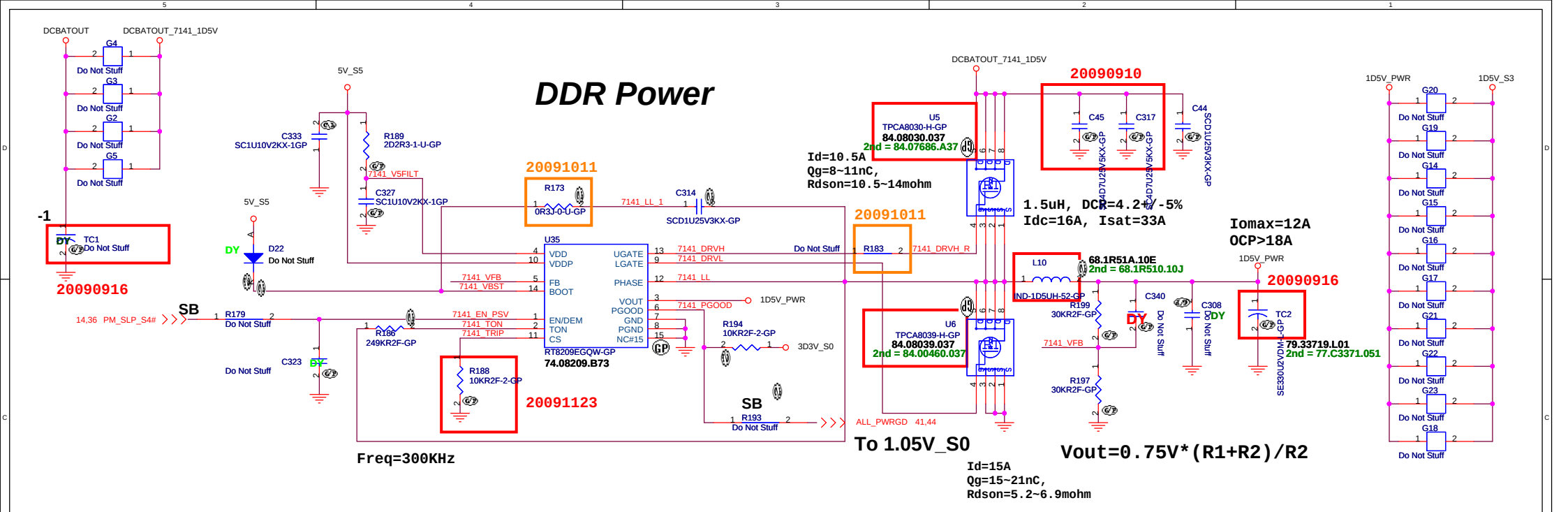
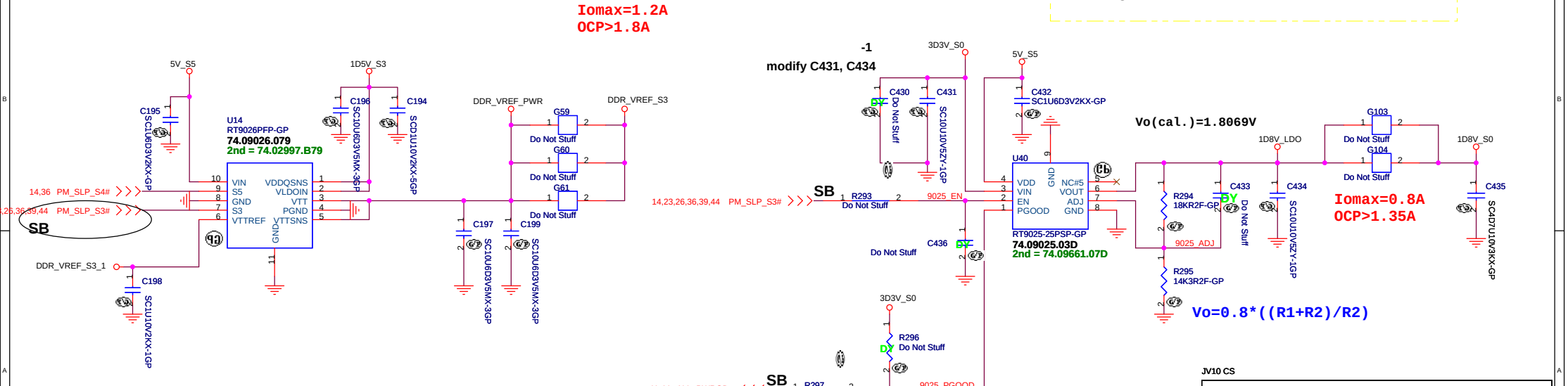


	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2



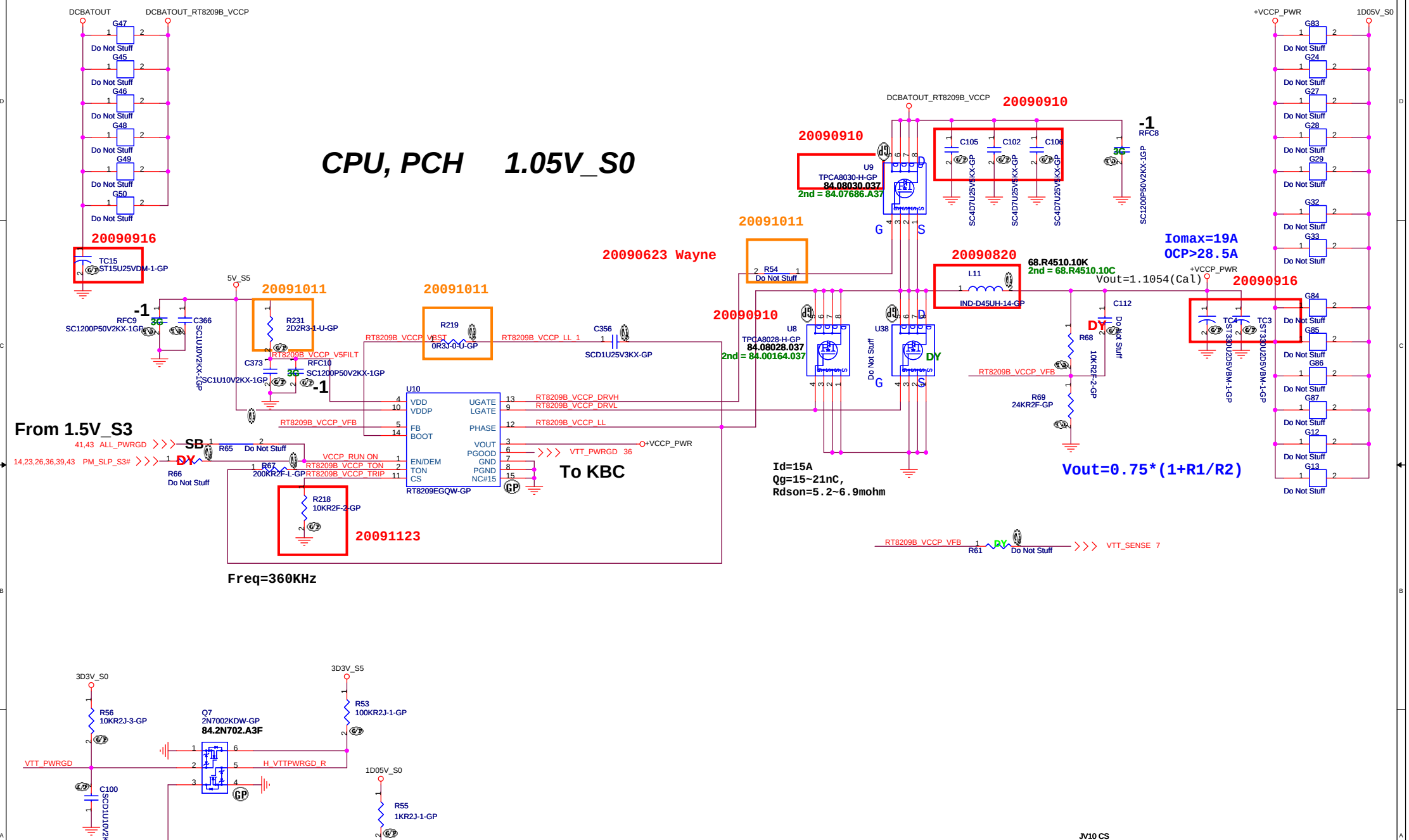
DDR_VREF_S3

RT9026 for DDR_VREF_S3_1



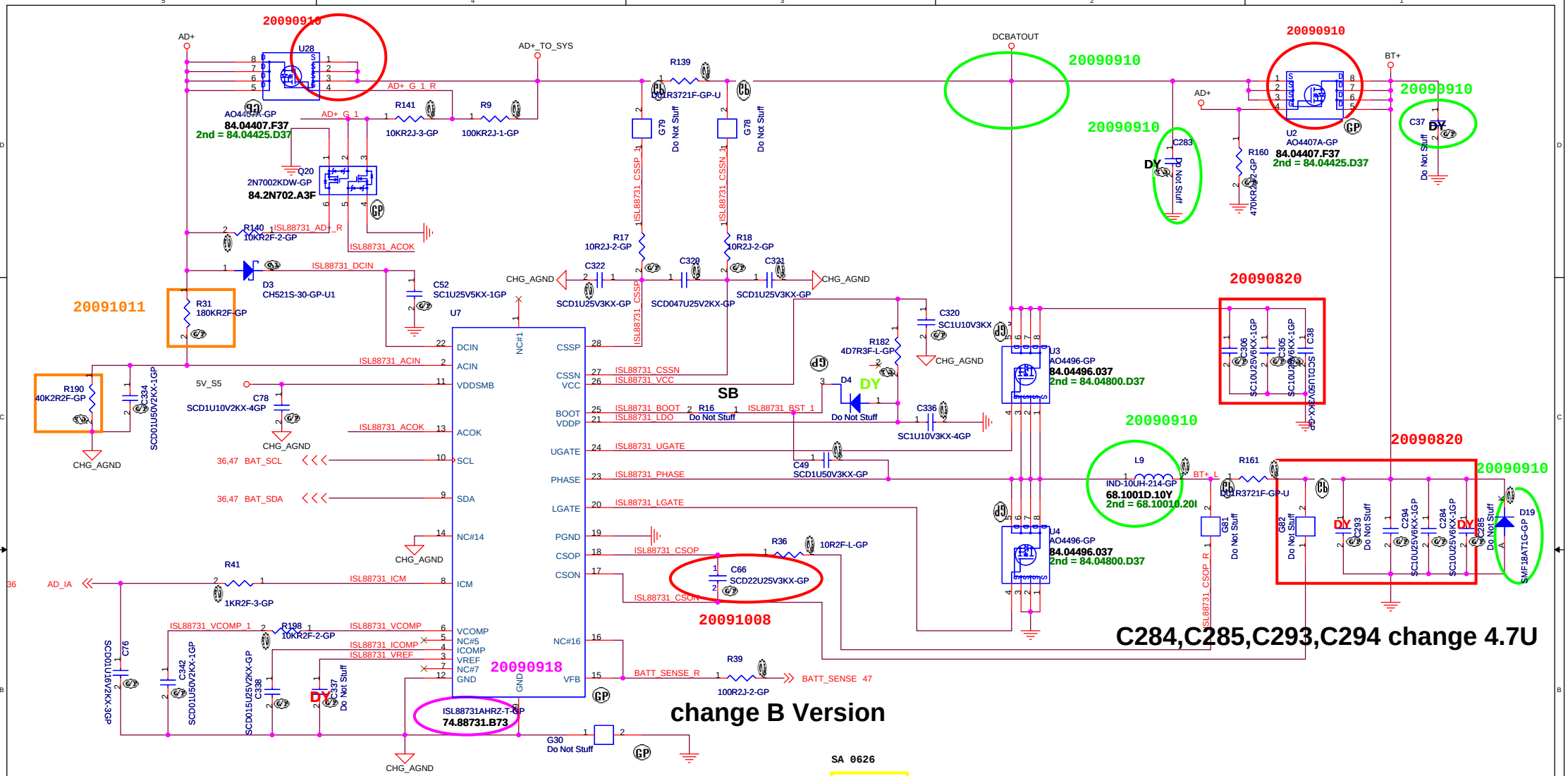
JV10 CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*RT8209E_1D5V_S3*	
Size	Document Number **JV10-CS**	Rev -1
Date: Friday, January 22, 2010	Sheet 43 of 50	

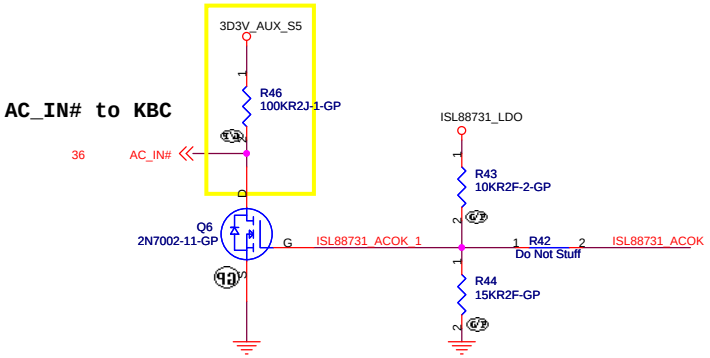


JV10 CS

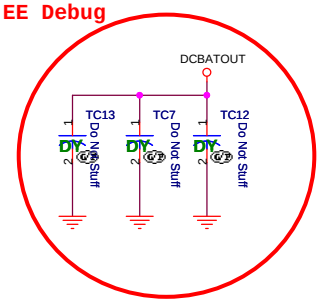
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RT8209B_1D05V_S0	
Size	Document Number JV10-CS	Rev -1
Date: Friday, January 22, 2010	Sheet 44 of 50	



SA 0626

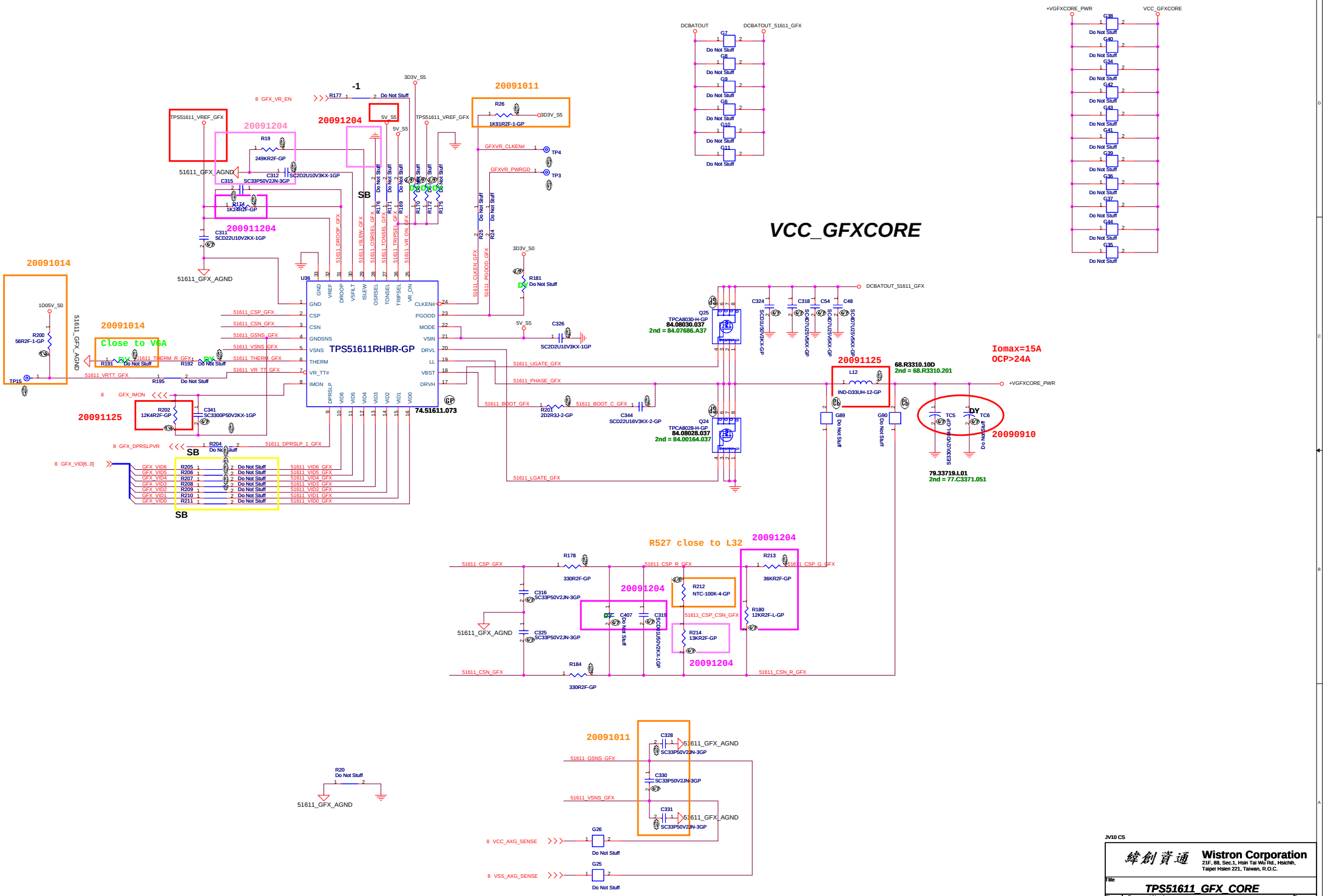


For EE Debug



JV10 CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ISL88731A CHARGER	
Size	Document Number: JV10-CS	Rev: -1
Date: Friday, January 22, 2010	Sheet 45 of 50	



JV10 CS

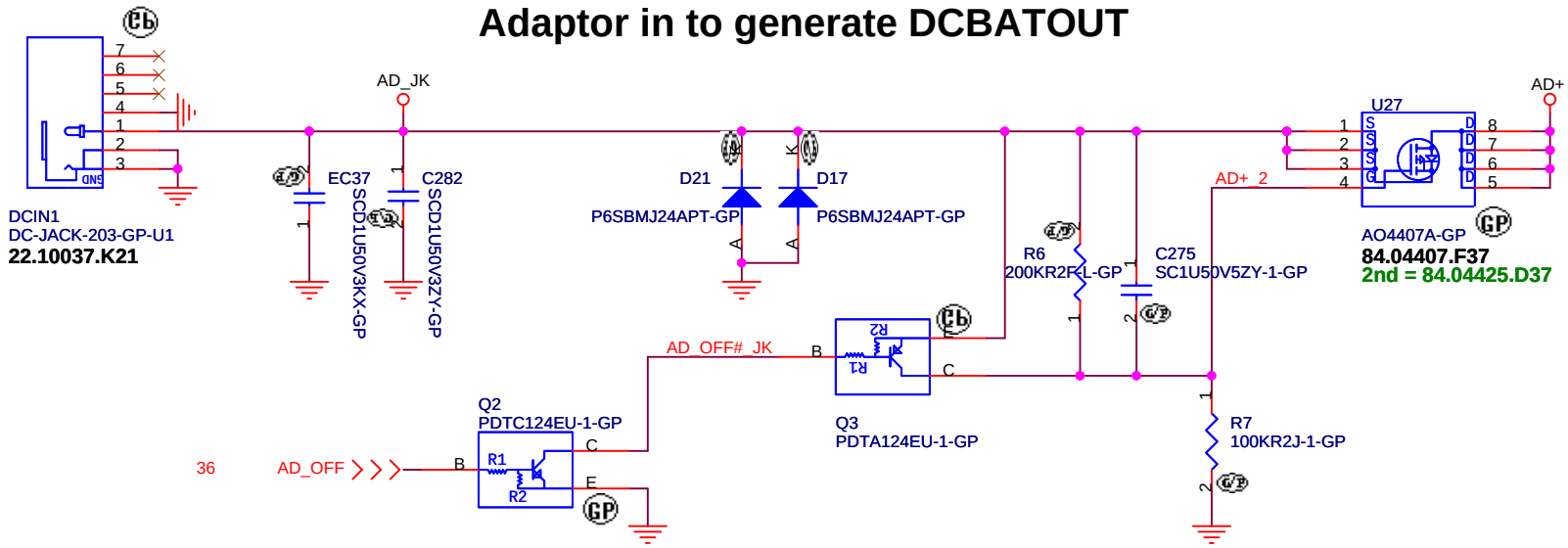
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51611_GFX_CORE**

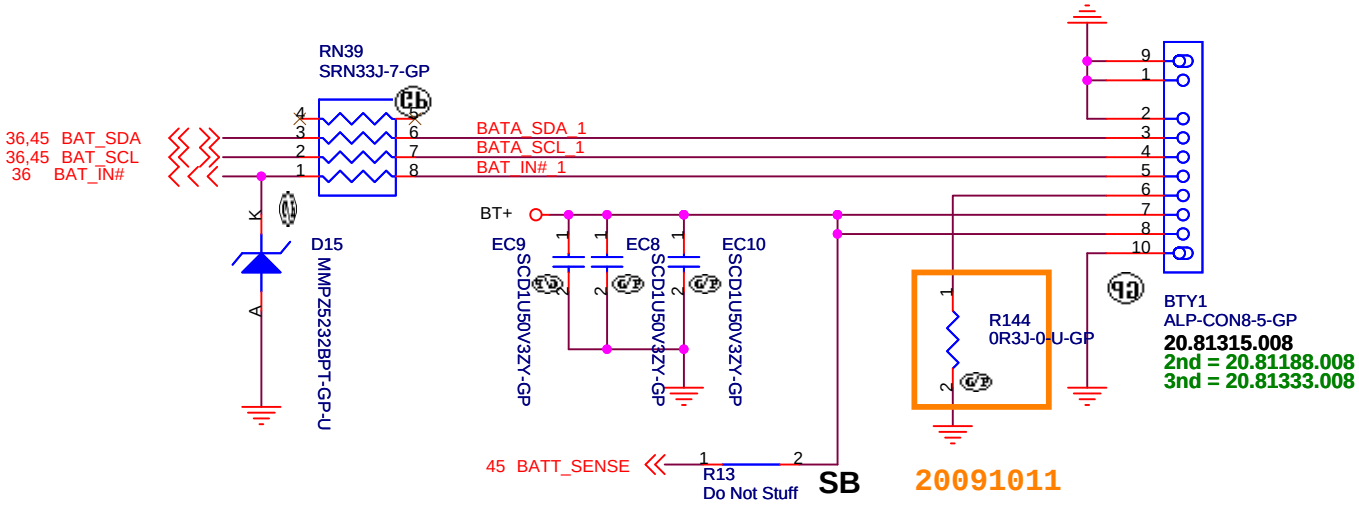
Size	Document Number	Rev
A2	JV10-CS	-1

Date: Friday, January 22, 2010 Sheet 46 of 50

Adaptor in to generate DCBATOUT



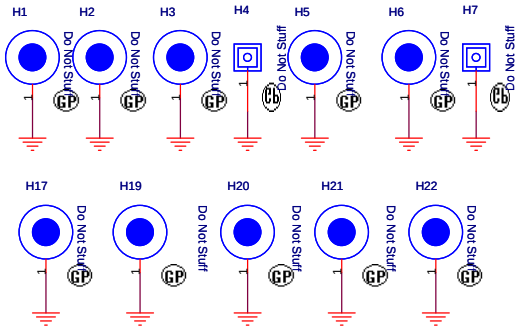
BATTERY CONNECTOR



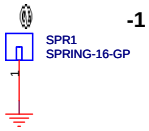
JV10 CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AD/BATT CONN**	
Size	Document Number **JV10-CS**	Rev **-1**
Date: Friday, January 22, 2010	Sheet 47 of 50	

MB HOLE



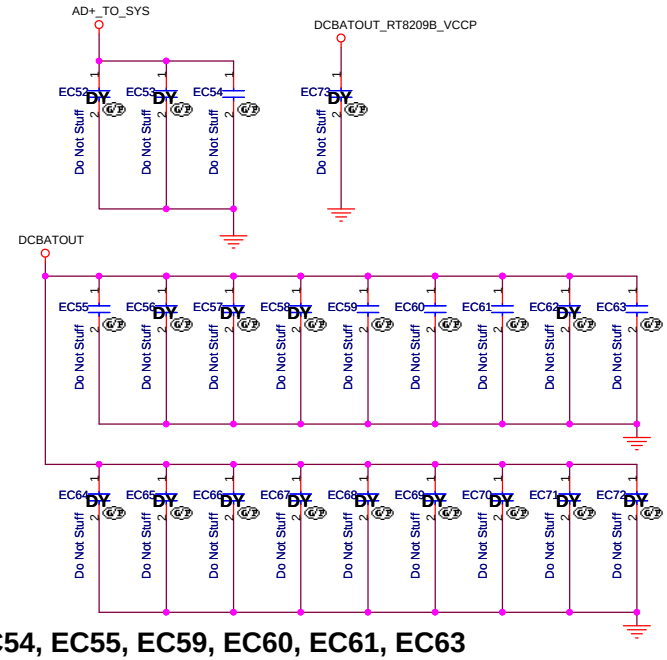
SPRING



-1

SB

EMI

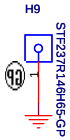


EC54, EC55, EC59, EC60, EC61, EC63

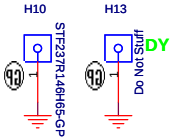
MINI CARD BOSS

(BTN Side)

HALF MINI CARD

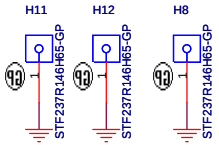


FULL MINI CARD

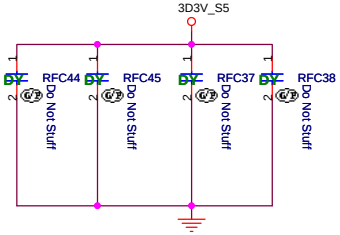


CPU PCH BOSS

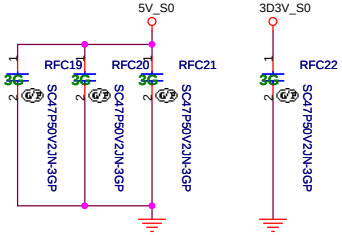
(BTN Side)



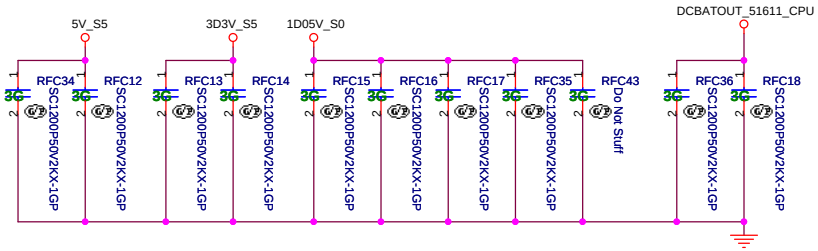
For RF power point Page 26



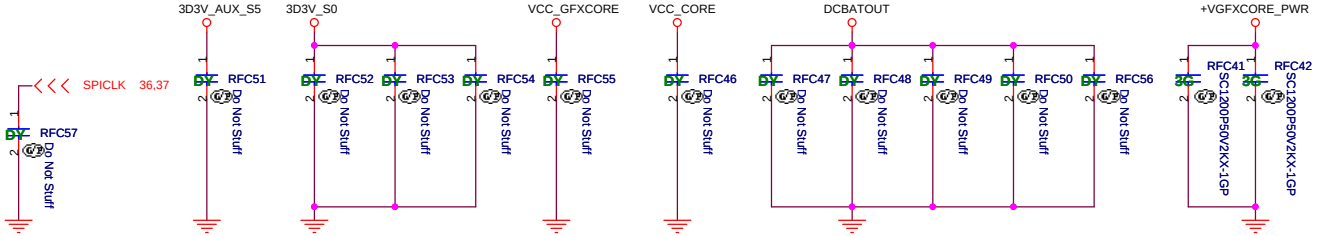
For RF power point Page 12



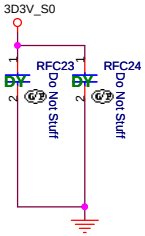
For RF power point Page 4

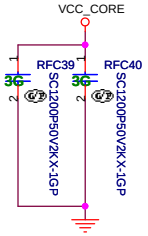


For RF power point Page 17



For RF power point Page 13





JV10 CS

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Title	EMI/Spring/Boss	
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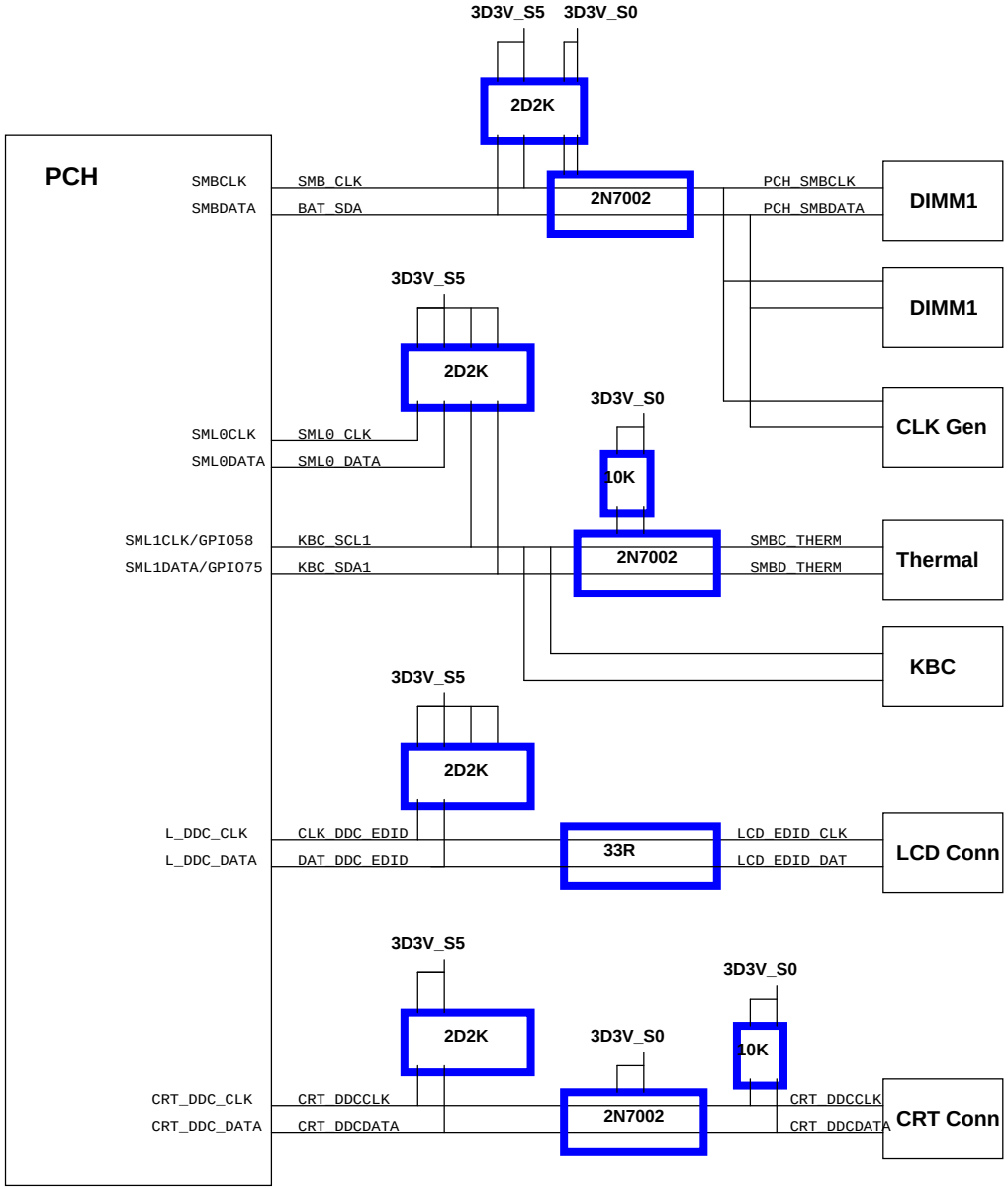
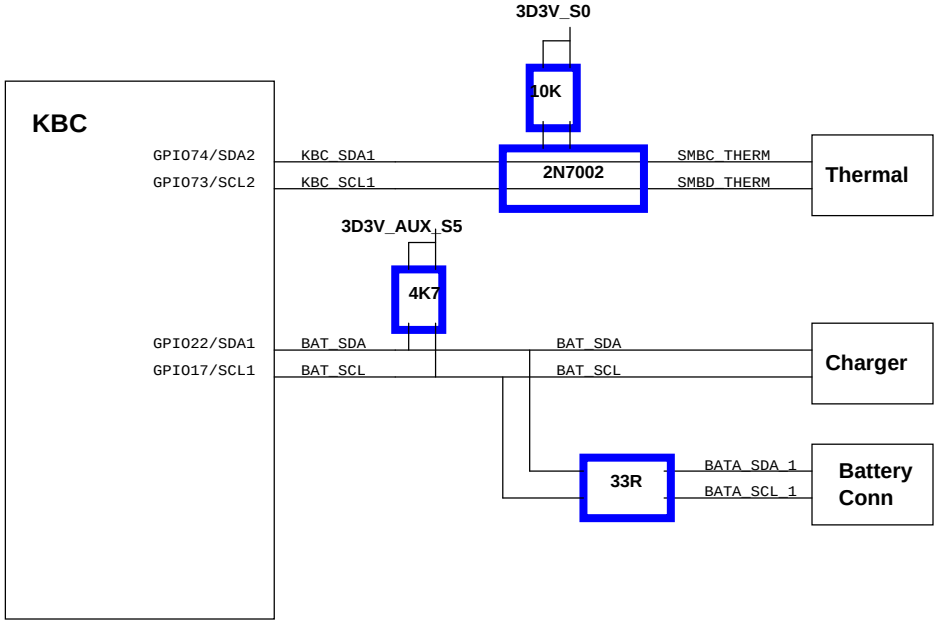
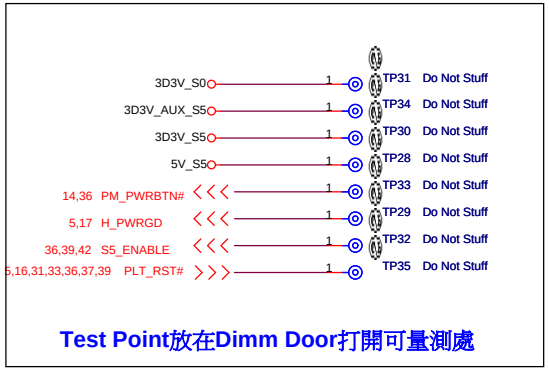
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Check test point



Test Point放在Dimm Door打開可量測處

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Title	AFTE_TP/SMB Diagram	
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SJM80 Schematic EC Tracking Record LAB 0325 , 2009
EC #/ Page / Description / Part Affected

EC SB11/04 add Intel support POC Function(power on current).
EC SB11/04 SWAP Touch Pad Pin define
EC SB11/04 R230 add 1K
EC SB11/04 change LOUT1 part number
EC SB11/11 SWAP Digital Mic DATA/CLK Pin define
EC SB11/11 Delete 3G_BTN#,Wireless_BTN#, function
EC SB11/11 add Cover switch to MB
EC SB11/11 add RN72 22ohm for Mic in
EC SB11/16 change U40 1D8V_S0 power solution
EC SB11/19 modify all LED off Function
EC SB11/19 change HDD Connector Type
EC SB11/19 Close Powert team Gap
EC PD 01/11 modify keyborad connector KB1
EC PD 01/11 modify USB Touch pad connector TPCN1 USBCN1
EC PD 01/11 add 3G module LED Function
EC PD 01/11 EMI add EC54, EC55, EC59, EC60, EC61, EC63, C37
EC PD 01/11 TPCN1 SWAP Pin define

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Title	Modify History	
Size A3	Document Number JV10-CS	Rev -1
Date: Friday, January 22, 2010	Sheet 50 of 50	