

Compal Confidential

VBL30/31

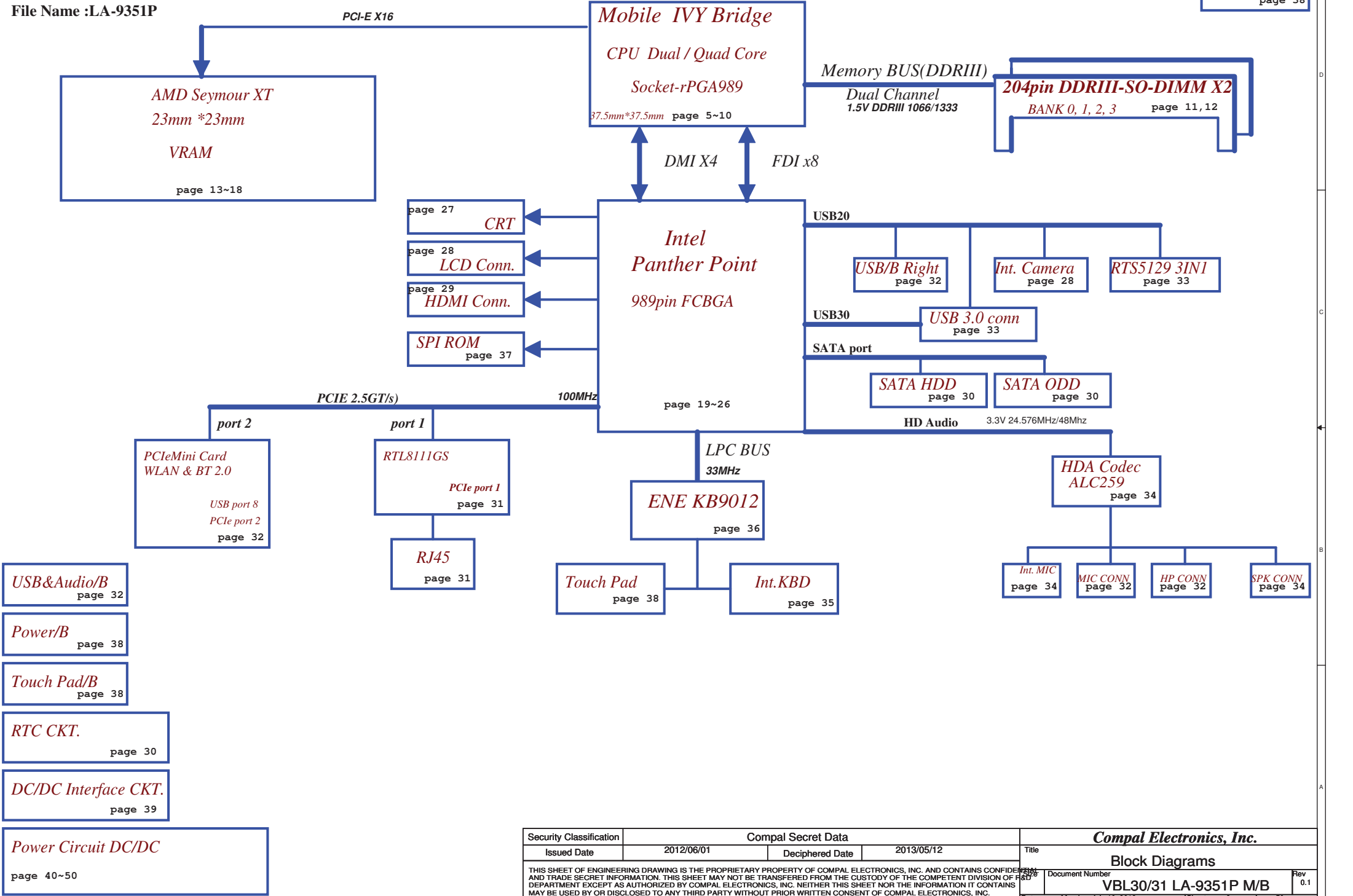
LA-9351P REV0.1 Schematic

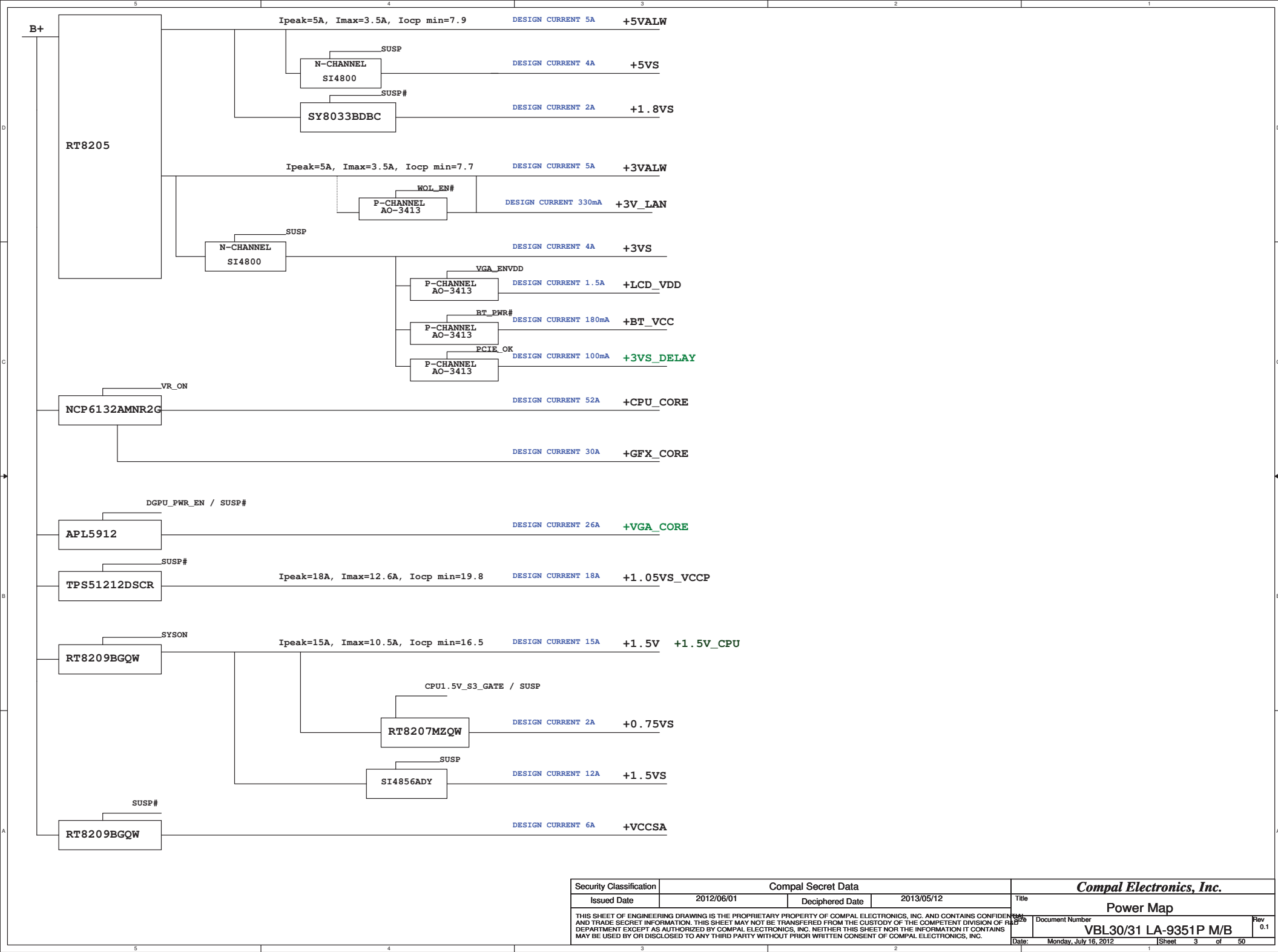
Intel Ivy Bridge/Panther Point

AMD Seymour XT

2012-05-08 Rev 0.1

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Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	Cover Page
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Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	Power Map	
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Voltage Rails

power plane	+B	+5VALW	+1.5V	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS
State		+3VALW	+1.5V_IO	
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

@	Reserve
CONN@	ME CONNECTOR
KB9012@	ENE EC
Nuvton@	Nuvton EC
NOW8@	not Support Win8
WIN8@	Support Win8
UMA@	UMA Sku
PX@	PX Sku

EC SM Bus1 address

Power	Device	Address
+3VALW	Smart Battery	0001 011x b

EC SM Bus2 address

Power	Device	Address
+3VS	VGA Internal thermal sensor	1001 111Xb (0x9E)

PCH SM Bus address

Power	Device	Address
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b

SMBUS Control Table

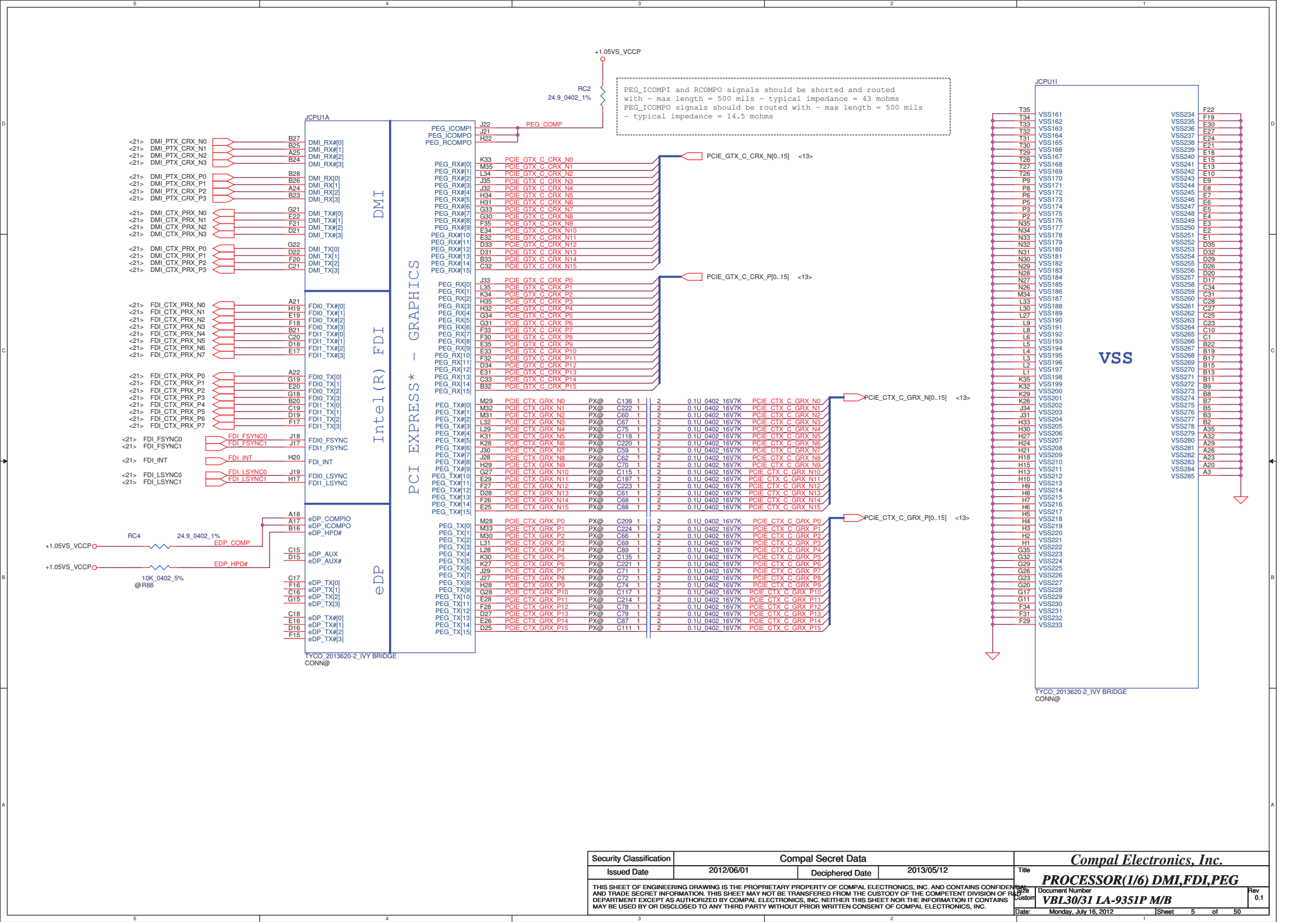
	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW	X	+3VALW	X	X	X	X	X
SMB_EC_CK2	KB9012	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW	X	X	X	X	X	X	+3VS
SMBCLK	PCH	X	X	X	V	V	X	X
SMBDATA	+3VALW	X	X	X	+3VS	+3VS	X	X
SML0CLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW	X	X	X	X	X	X	X
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VS	X	+3VS	X	X	+3VS	X

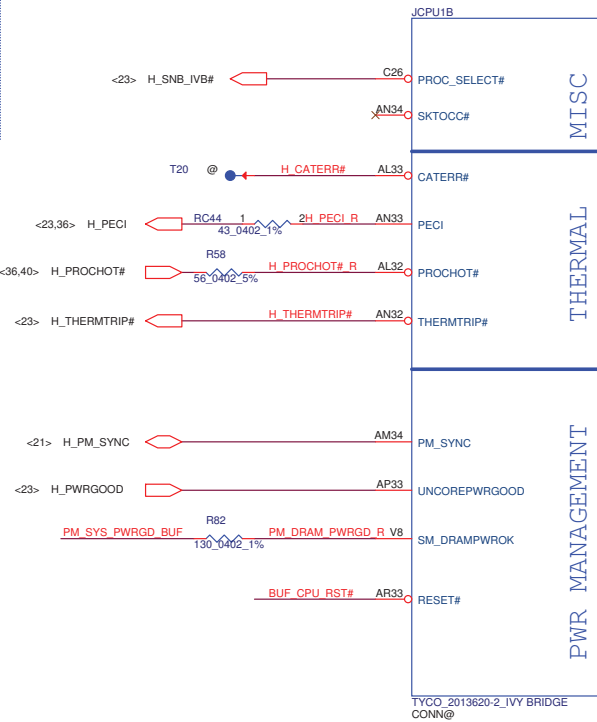
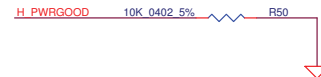
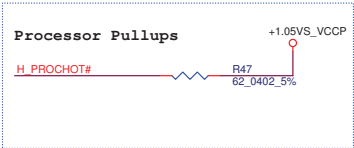
PCH X76 and PCBA table

		config
X76	ZZZ X76@ HYN 1G	ZZZ @ HYN 1G R359 @ 10K_0402_5% R361 @ 10K_0402_5% R462 @ 10K_0402_5%
	ZZZ X76@ SAM 1G	ZZZ @ SAM 1G R360 @ 10K_0402_5% R361 @ 10K_0402_5% R461 @ 10K_0402_5%
PCH	UH1 BD82HM70 QPXH C1 BGA 989P PCH@	
PCB	ZZZ DAZ@ PCB LA-6732P REV10	ZZZ DA8@ PCB LA-9351P REV01
	ZZZ DA4@ PCB LS-6732P REV10	ZZZ DA2@ PCB LS-6731P REV10

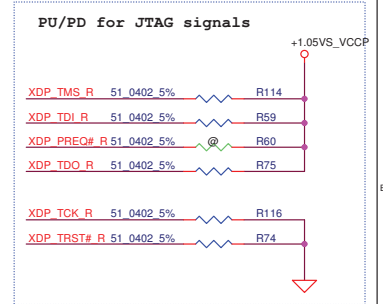
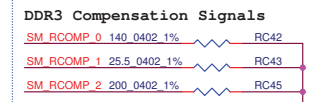
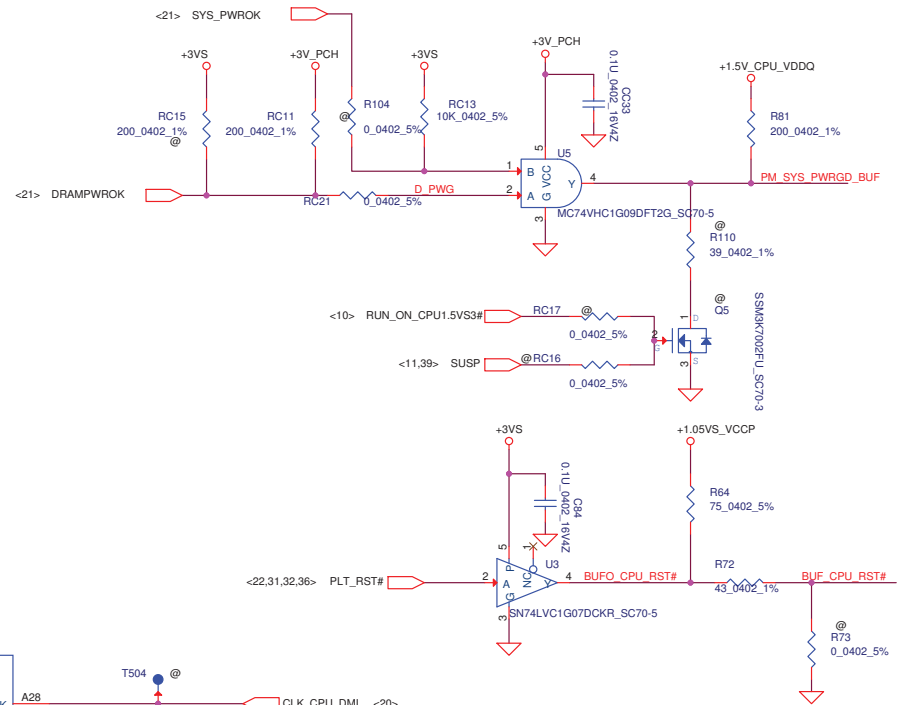
(@/CONN@/DA2@/DA4@/DA8@/DAZ@/KB9012@/NOW8@/Nuvton@/PCH@/PX@/Rev01@/Rev02@/Rev03@/Rev04@/Rev10@/UMA@/WIN8@/X76@)

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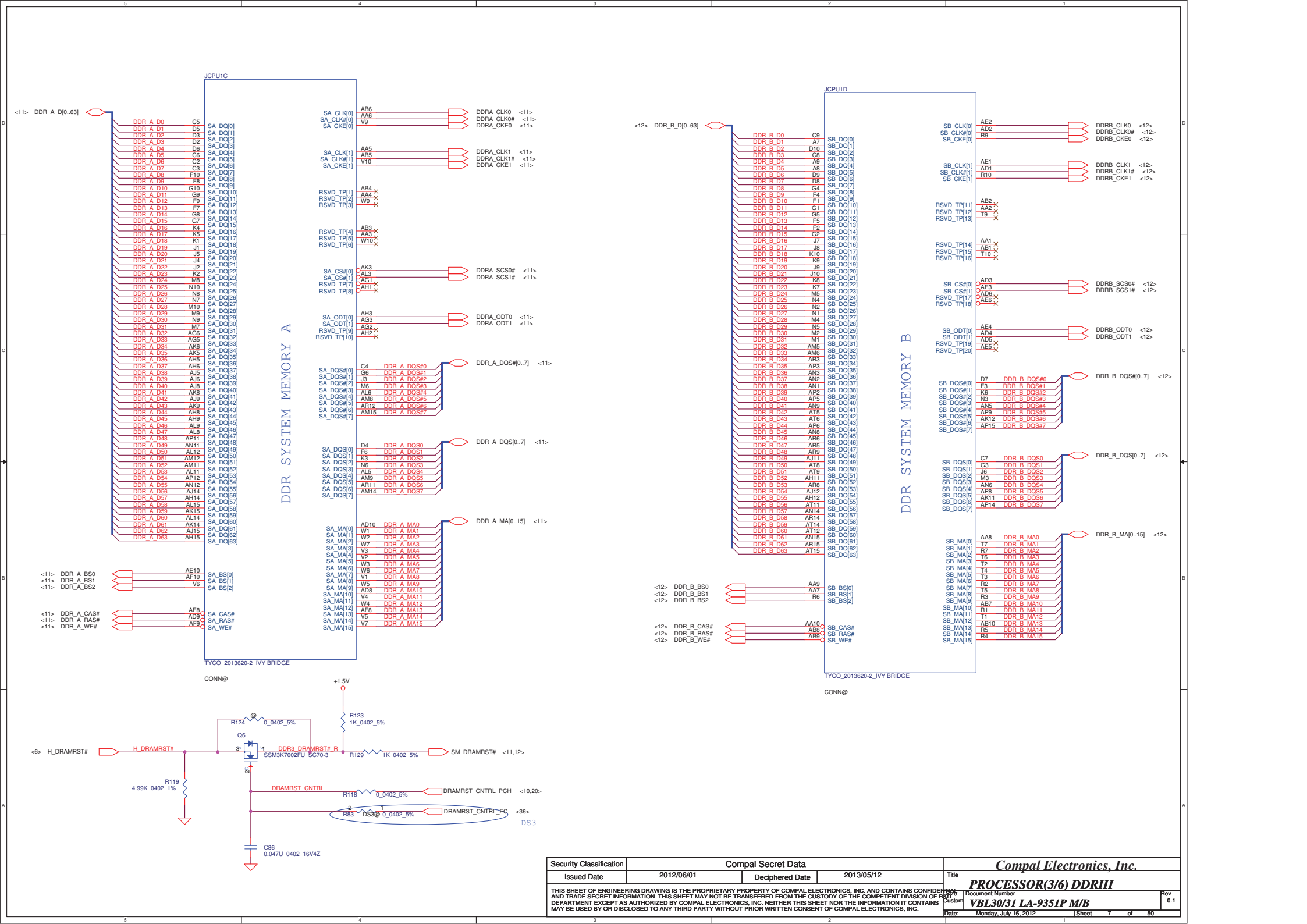




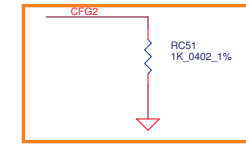
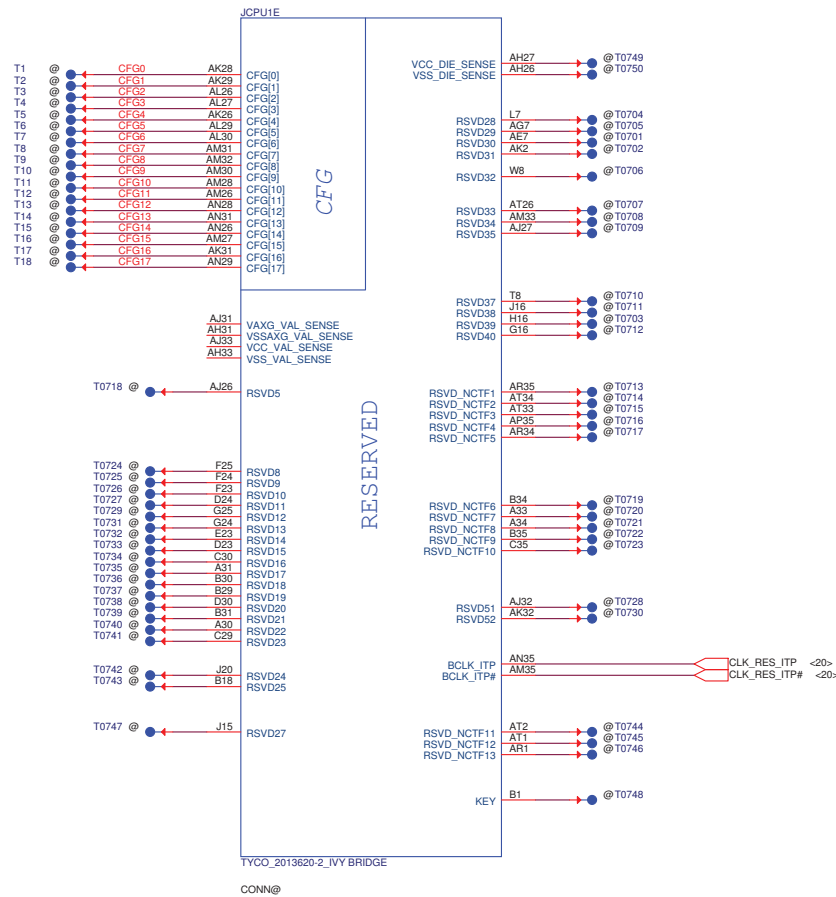
TYCO_2013620-2_IVY BRIDGE
CONN@



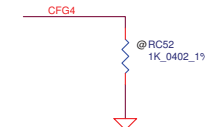
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				PROCESSOR(2/6) PM,XDP,CLK	
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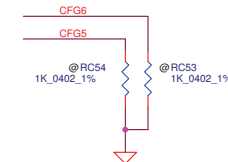
CFG Straps for Processor



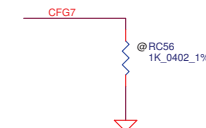
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



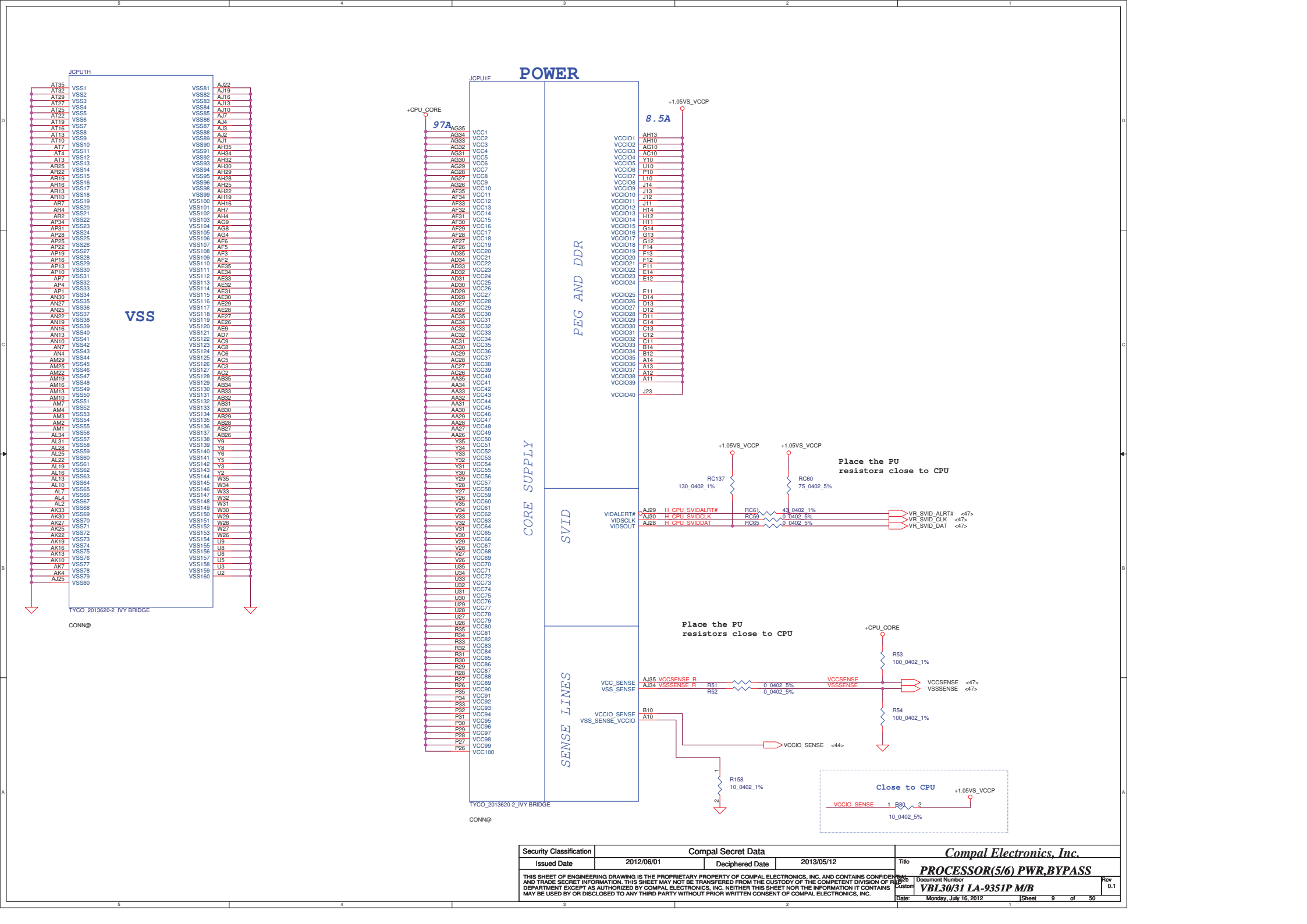
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

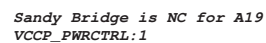
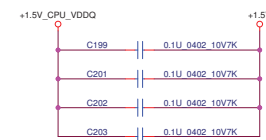
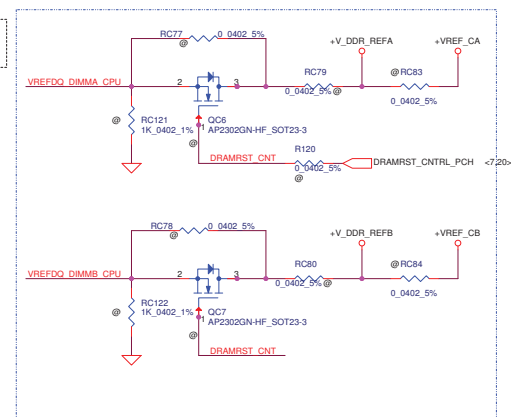


PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

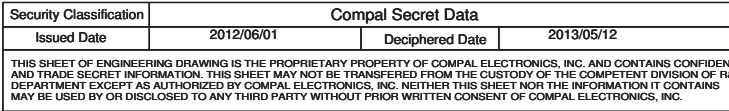


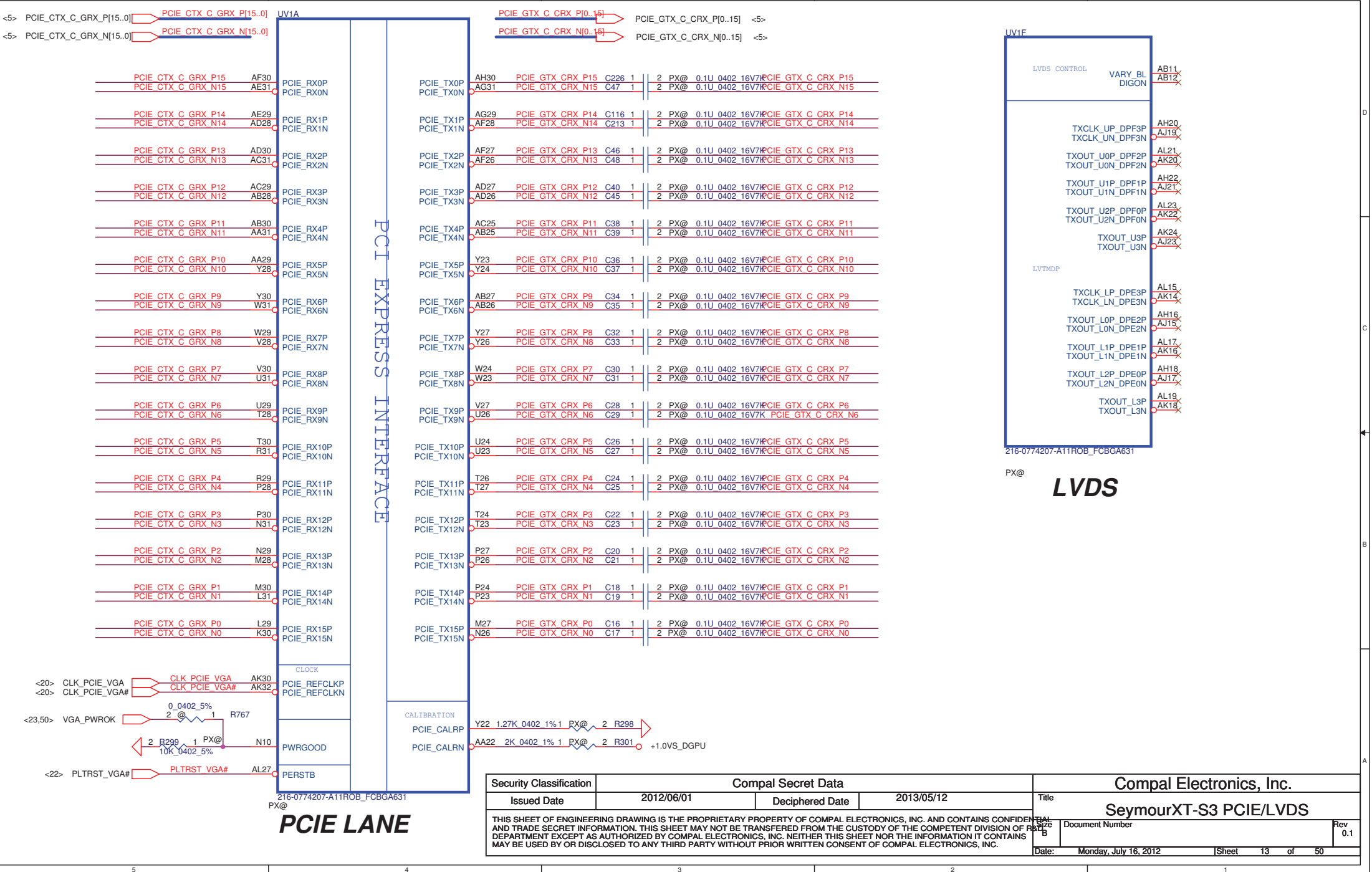
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training



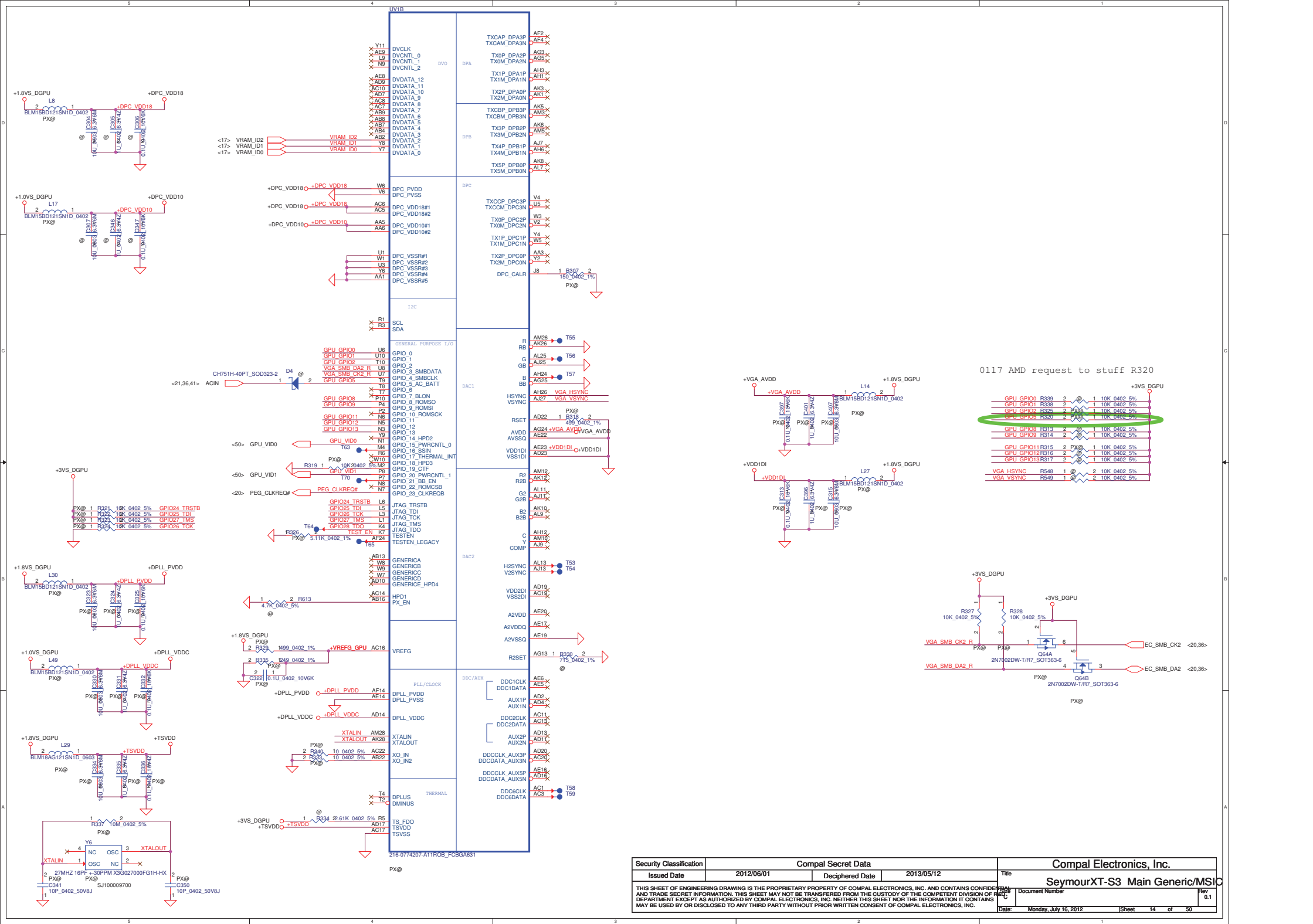


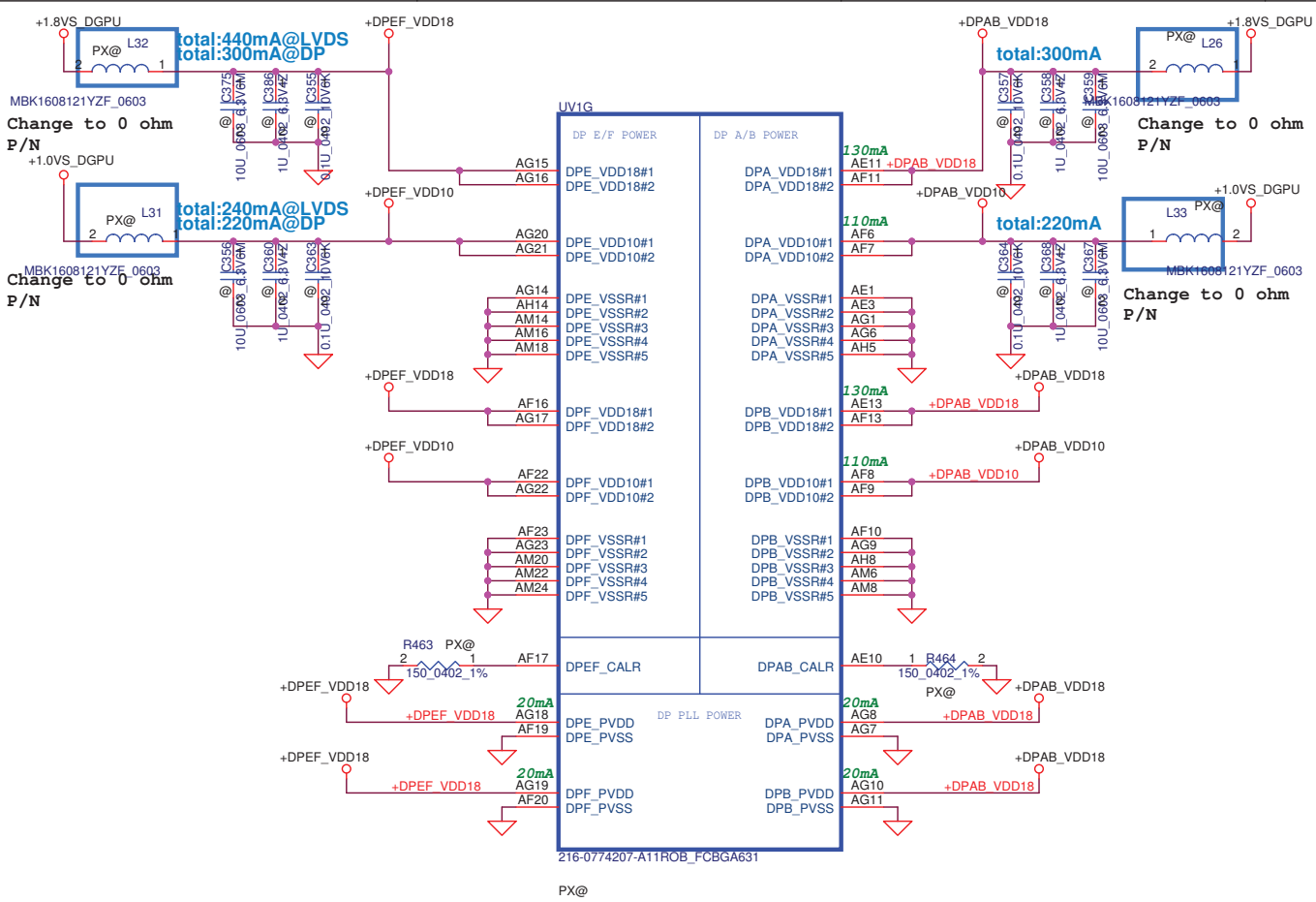
Security Classification	Compal Secret Data		Title	<i>Compal Electronics, Inc.</i>	
Issued Date	2016/06/01	Deciphered Date	2013/05/12	PROCESSOR(6/6) PWR,VSS	
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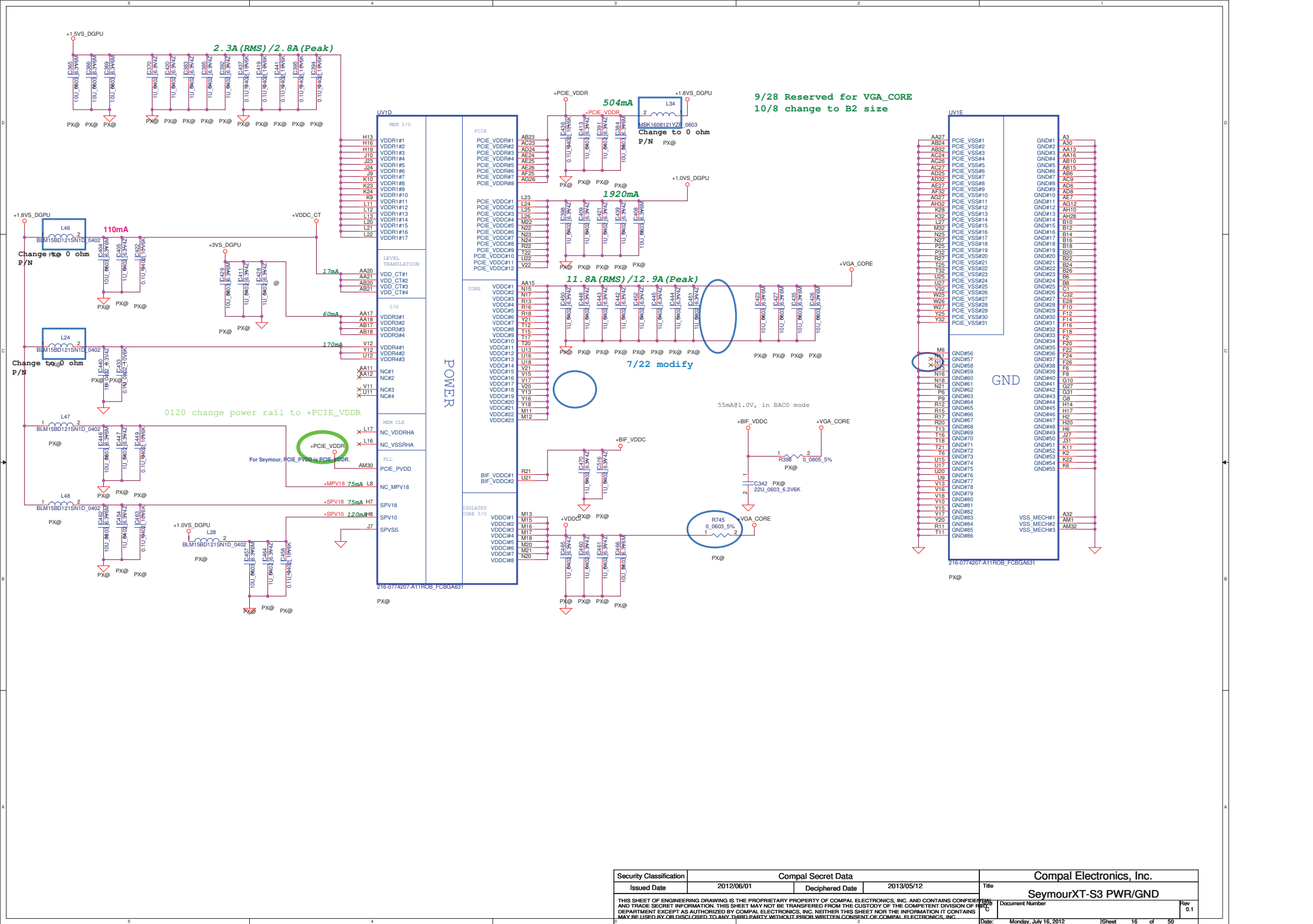


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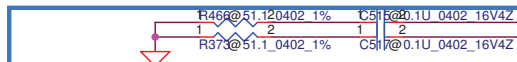
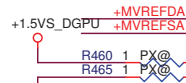
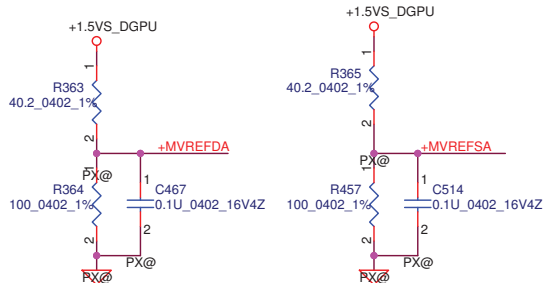
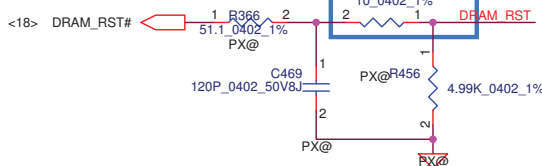
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PARK SCL has
different recommend

9/28 change P/N to
SD034100A80



Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observation,if
not need, DNI.

M DA0 K27
M DA1 J29
M DA2 H30
M DA3 H32
M DA4 G29
M DA5 F28
M DA6 F32
M DA7 F30
M DA8 C30
M DA9 F27
M DA10 A28
M DA11 C28
M DA12 E27
M DA13 G26
M DA14 D26
M DA15 F25
M DA16 A25
M DA17 C25
M DA18 E25
M DA19 D24
M DA20 E23
M DA21 F23
M DA22 D22
M DA23 F21
M DA24 E21
M DA25 D20
M DA26 F19
M DA27 A19
M DA28 D18
M DA29 F17
M DA30 A17
M DA31 C17
M DA32 E17
M DA33 D16
M DA34 F15
M DA35 A15
M DA36 D14
M DA37 F13
M DA38 A13
M DA39 C13
M DA40 E11
M DA41 A11
M DA42 C11
M DA43 F11
M DA44 A9
M DA45 C9
M DA46 F9
M DA47 D8
M DA48 E7
M DA49 A7
M DA50 C7
M DA51 F7
M DA52 A5
M DA53 E5
M DA54 C3
M DA55 E1
M DA56 G7
M DA57 G6
M DA58 G1
M DA59 G3
M DA60 J6
M DA61 J1
M DA62 J3
M DA63 J5

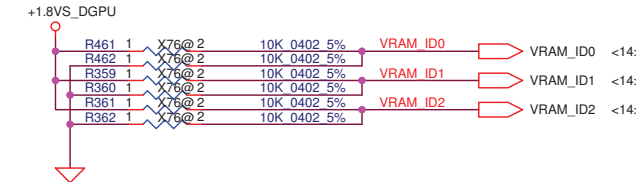
MEMORY
INTERFACE

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DDBIA1_2/WDQSA_6
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ADBIA1/ODTA1
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CLKA0B
CLKA1
CLKA1B
RASA0B
RASA1B
CASA0B
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WEA1B

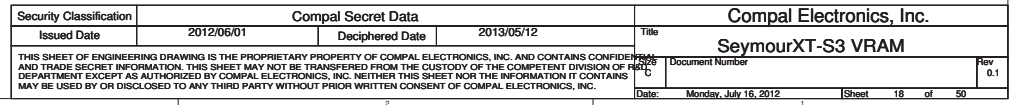
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CSA1B_1
CKEA0
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WEA0B
WEA1B

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M MA1
M MA2
M MA3
M MA4
M MA5
M MA6
M MA7
M MA8
M MA9
M MA10
M MA11
M MA12
M BA2
M BA0
M BA1
M DQM0
M DQM1
M DQM2
M DQM3
M DQM4
M DQM5
M DQM6
M DQM7
M DQS0
M DQS1
M DQS2
M DQS3
M DQS4
M DQS5
M DQS6
M DQS7
M DQS#0
M DQS#1
M DQS#2
M DQS#3
M DQS#4
M DQS#5
M DQS#6
M DQS#7
VRAM_ODT0
VRAM_ODT1
M_CLK0
M_CLK#0
M_CLK1
M_CLK#1
M_RAS#0
M_RAS#1
M_CAS#0
M_CAS#1
M_CS#0
M_CS#1
M_CKE0
M_CKE1
M_WE#0
M_WE#1



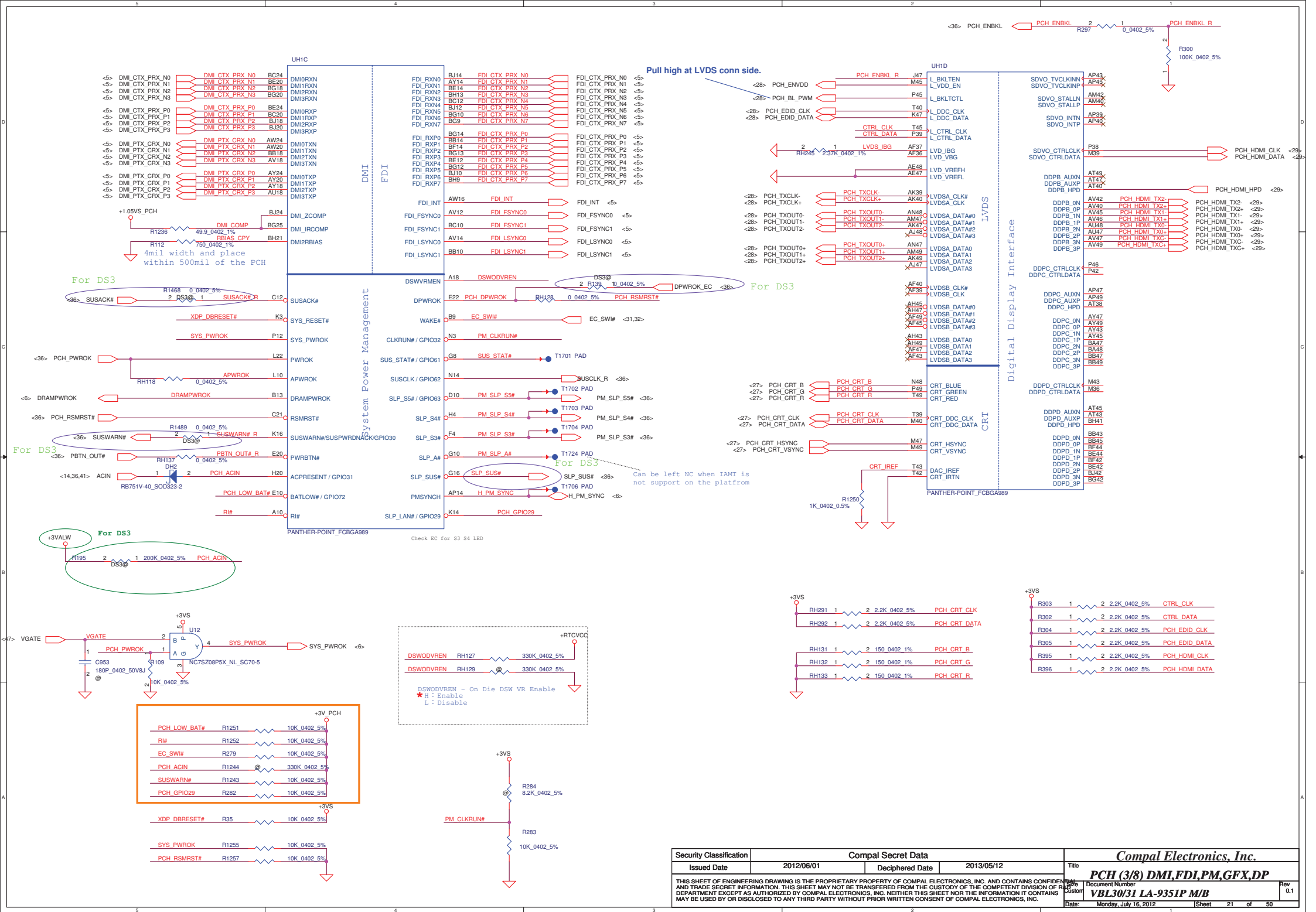
Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
K4W1G1646G-BC11 Samsung 128MB PN:SA00004GS00	R461	R360	R362
H5TQ1G63DFR-11C Hynix 128MB PN:SA000041S20	R462	R359	R362
K4W2G1646C-BC11 Samsung 256MB PN:SA000047Q00	R461	R360	R361
H5TQ2G63BFR-11C/H5TQ2G63DFR-11C Hynix 256MB PN:SA00003YO10/ SA00003YOA0	R462	R359	R361

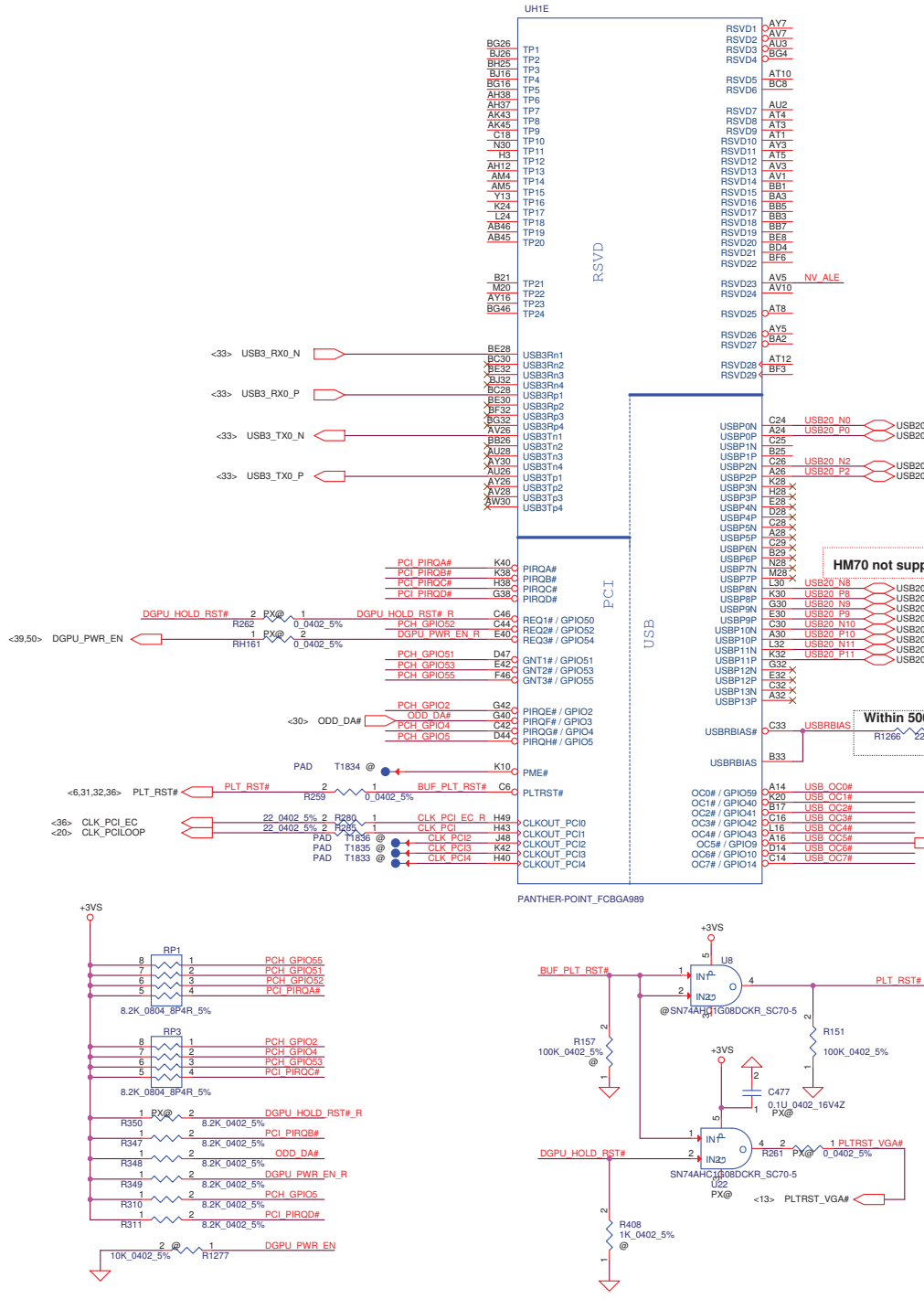
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title
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				Document Number
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Security Classification	Compal Secret Data			Compal Electronics, Inc.			
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	PCH (2/8) PCIE, SMBUS, CLK		
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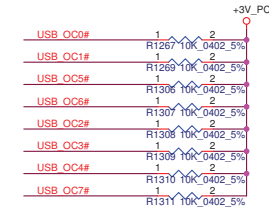
GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

Boot BIOS Strap		
BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved(NAND)
1	0	Reserved
1	1	SPI ★

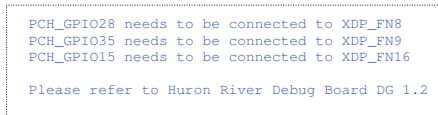
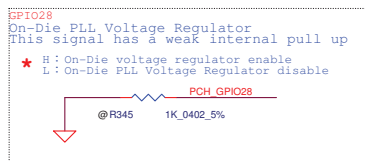
Intel Anti-Theft Technology	
NV_ALE	High=Enabled
	Low=Disable(Floating) ★

NV_ALE @R341 1K 0402 5% +1.8VS

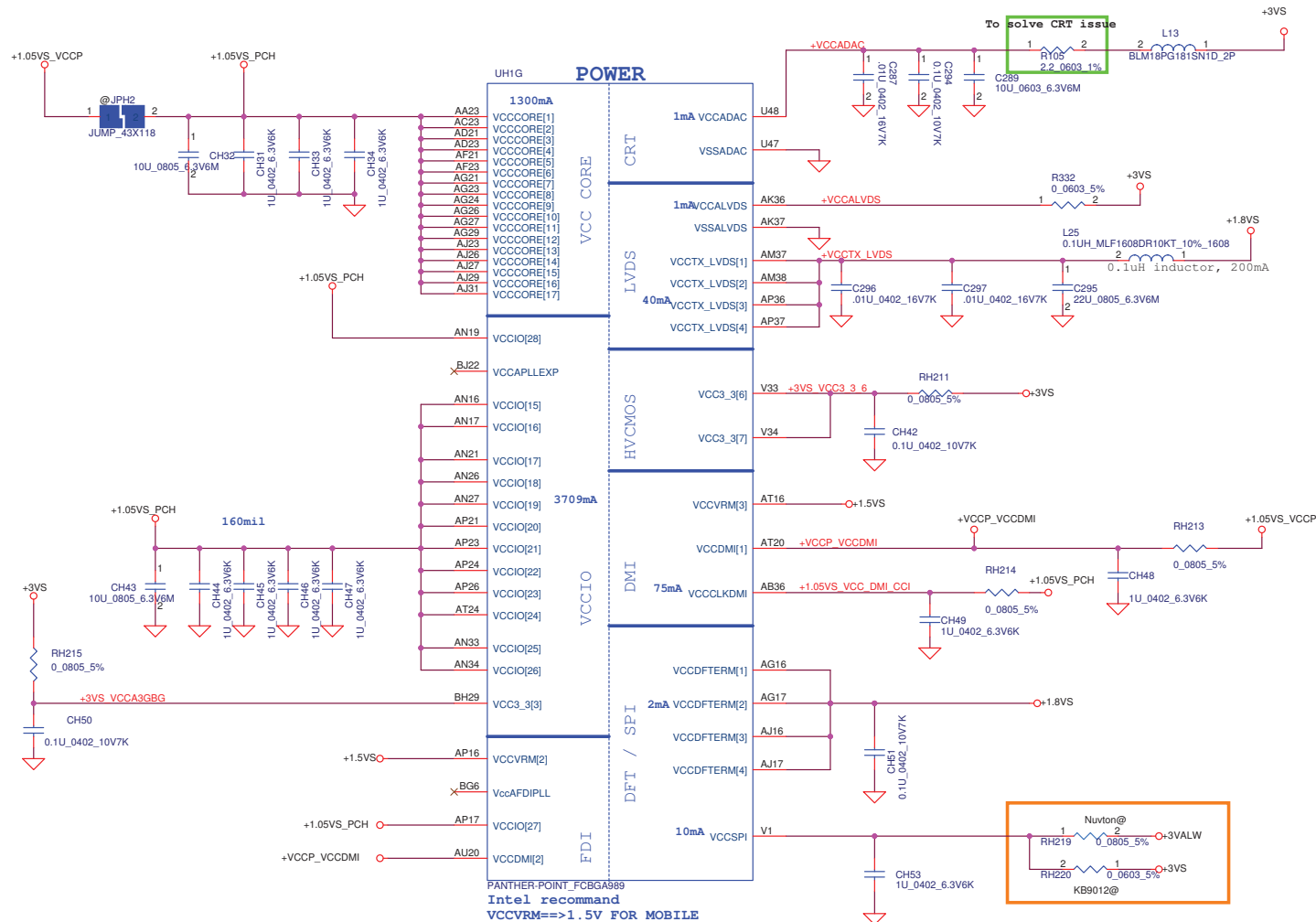
HM70 not support USB port 4,5,6,7,12,13



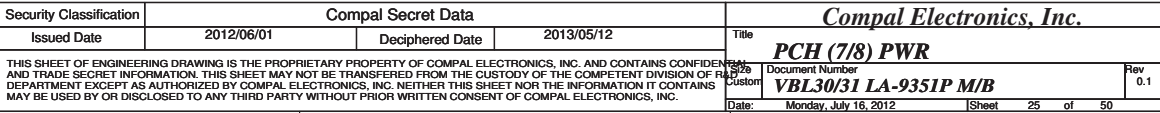
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	PCH (4/8) PCI, USB, NVRAM
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				Sheet	22 of 50

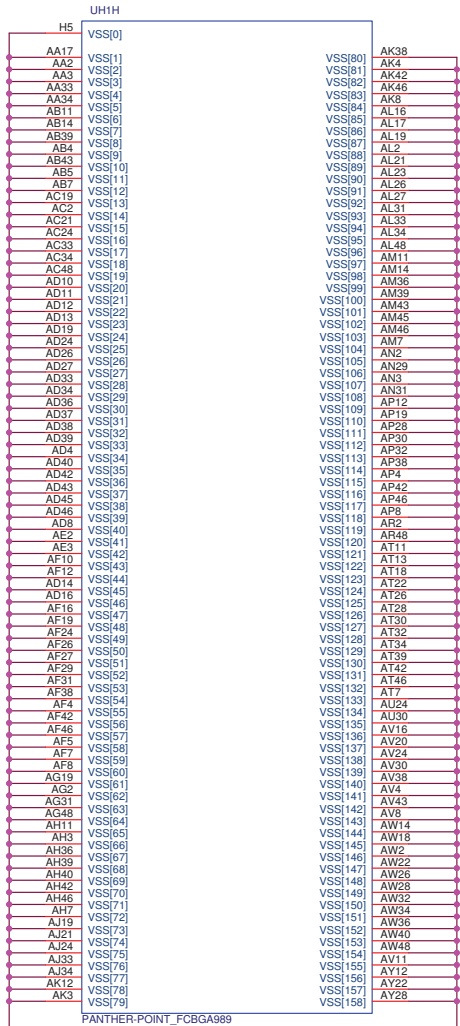


Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> PCH (5/8) GPIO, CPU, MISC	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	Rev 0.1
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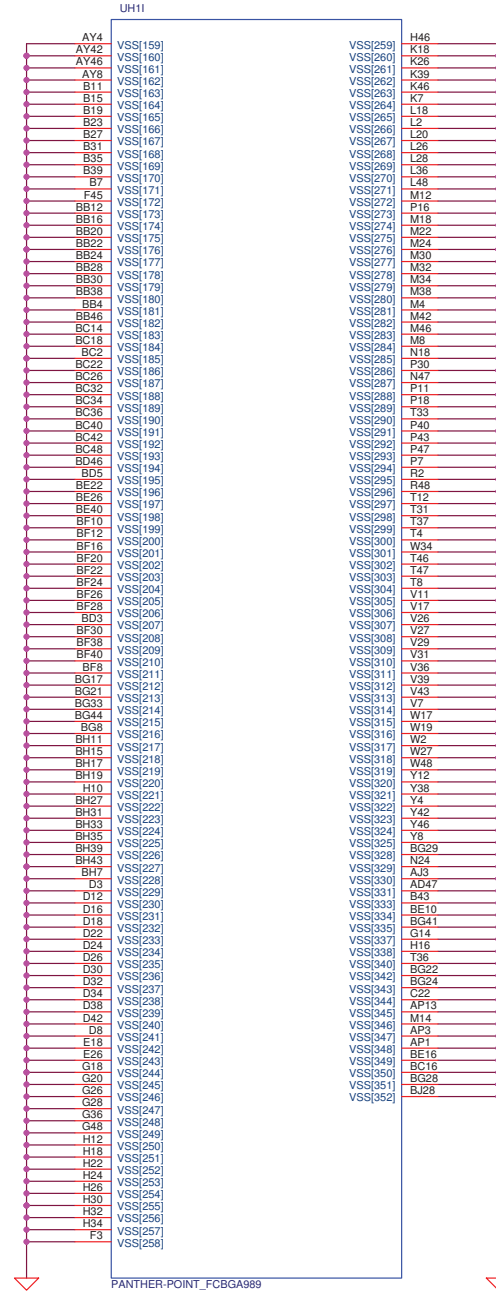


PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



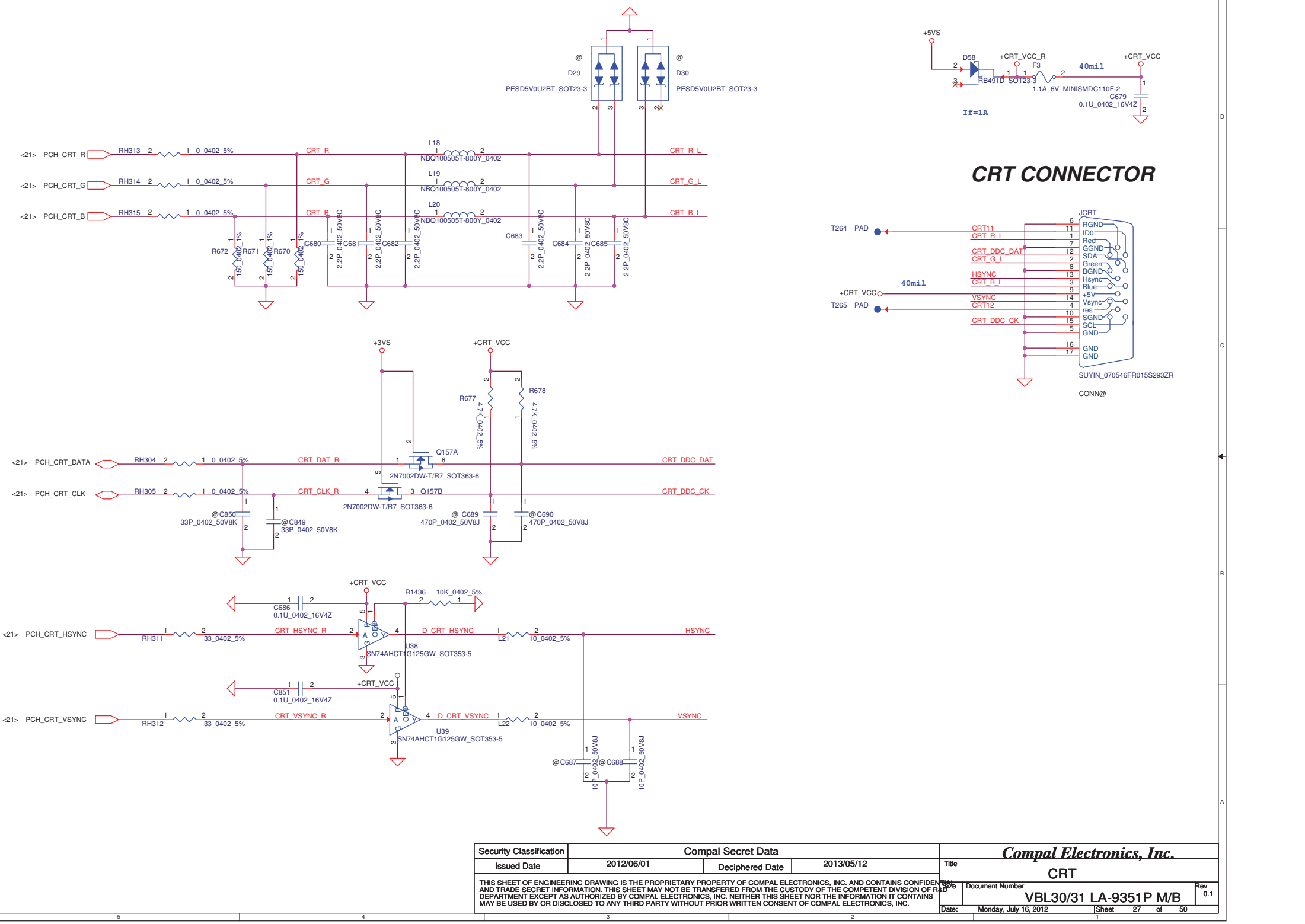


PANTHER-POINT_FCBGA989



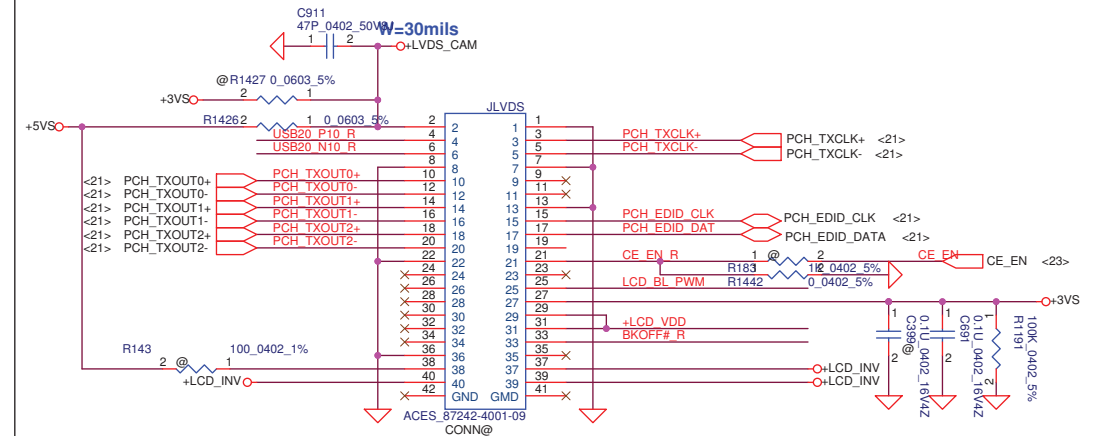
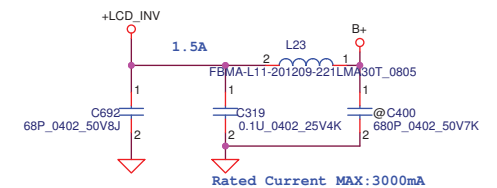
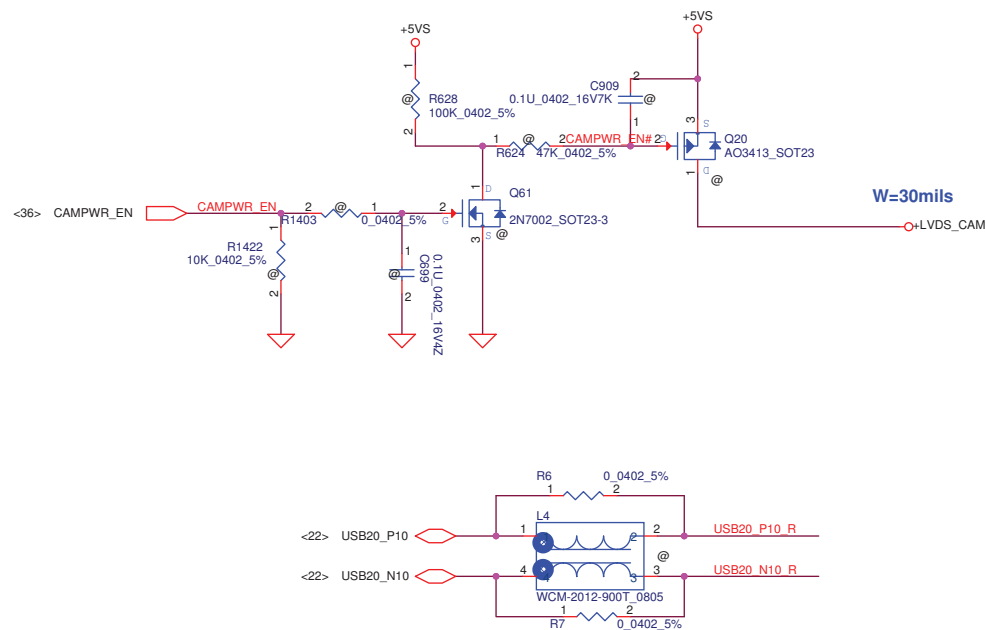
PANTHER-POINT_FCBGA989

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Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	PCH (8/8) VSS
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				Document Number	VBL30/31 LA-9351P M/B
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				Sheet	26 of 50

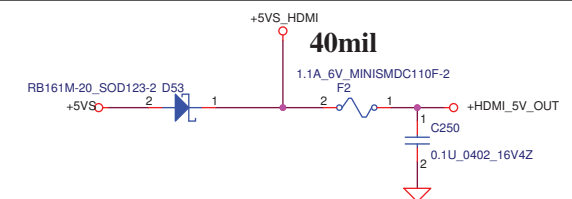
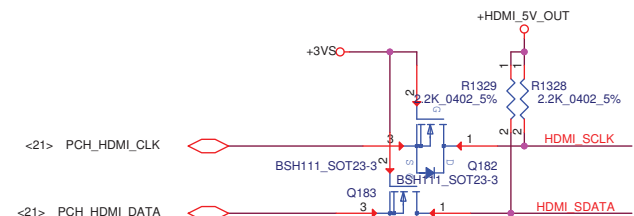
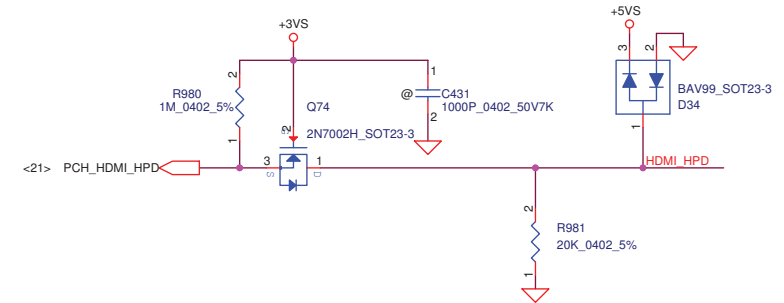
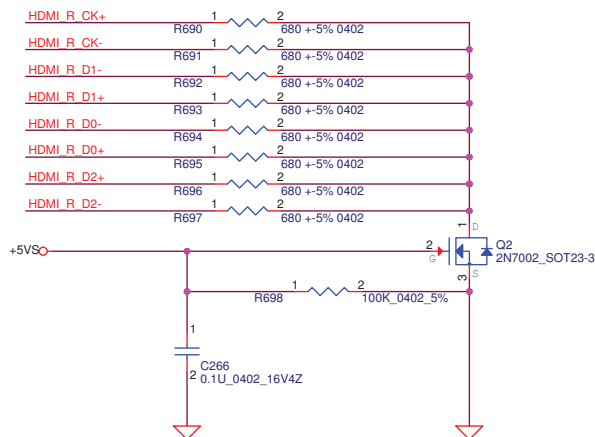
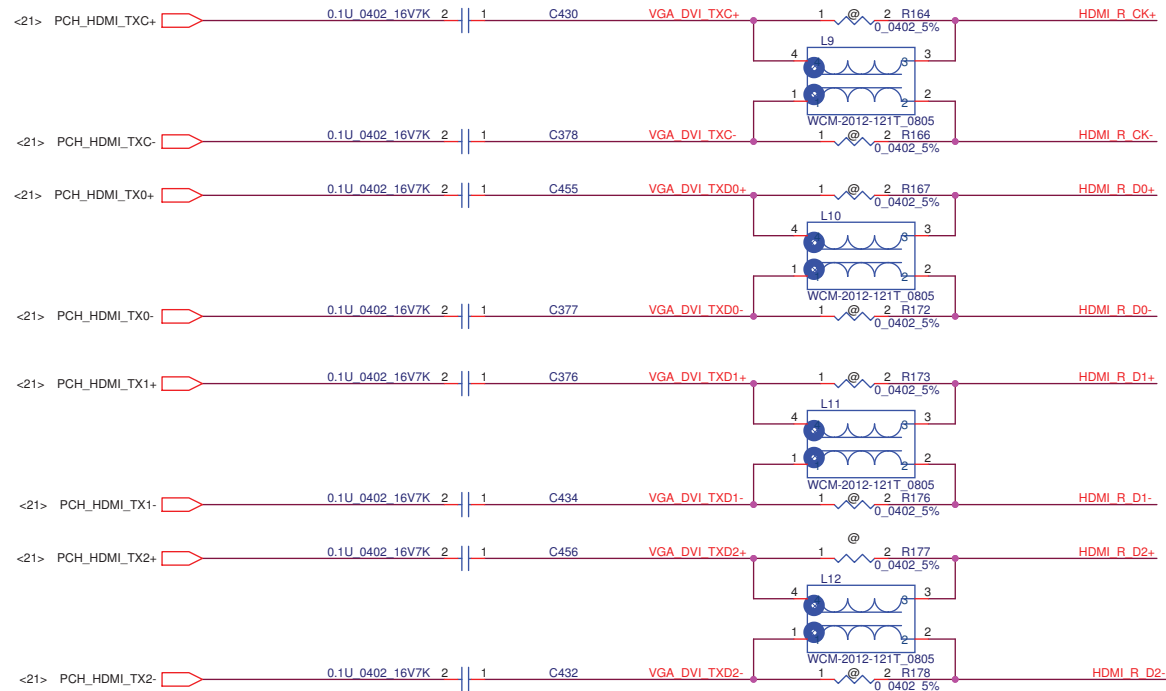


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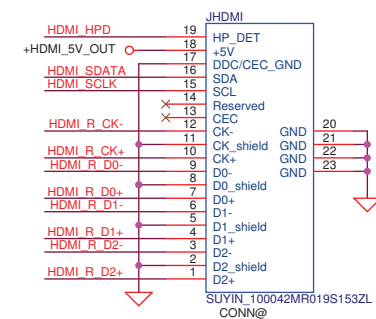
LCD POWER CIRCUIT

[illegible]**LCD/PANEL BD. Conn.**

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Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	LVDS		
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				Date:	Monday, July 16, 2012		Sheet 28 of 50

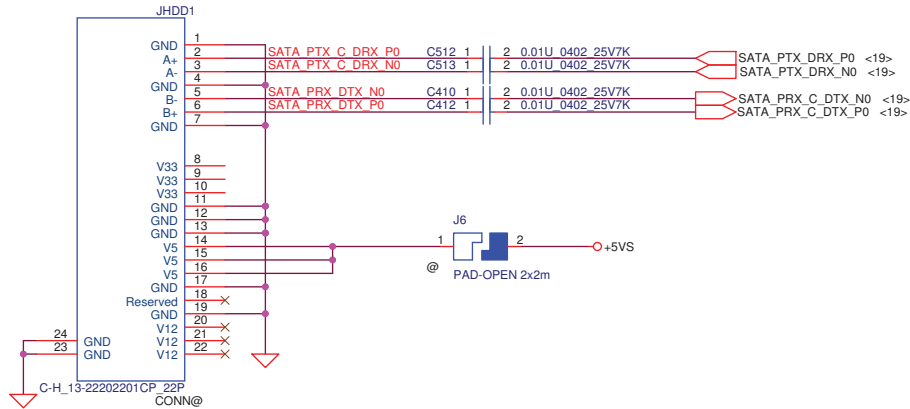
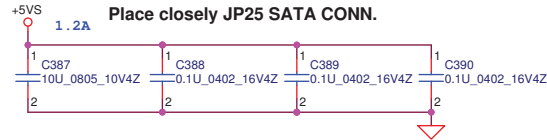


HDMI Connector

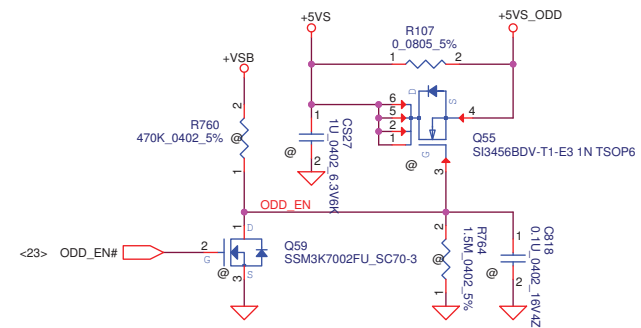
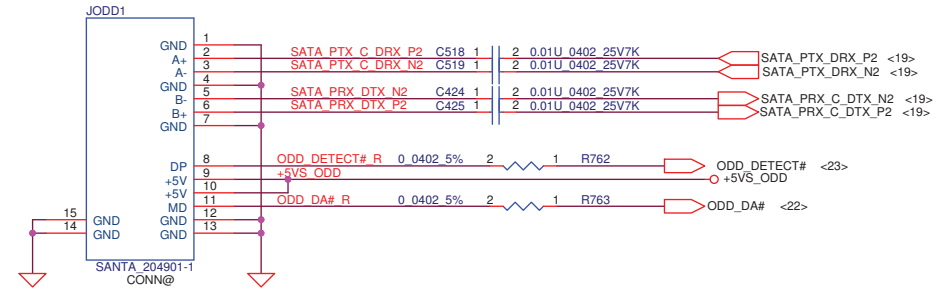
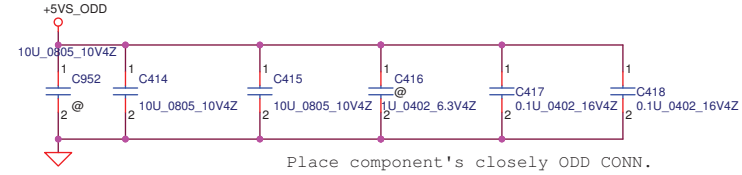


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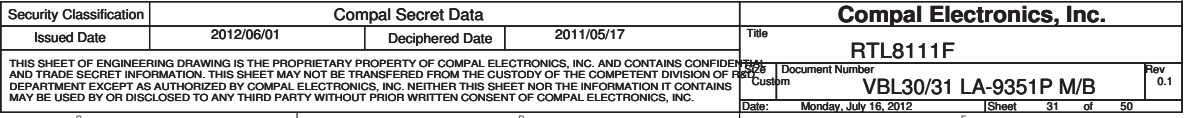
SATA HDD1 Conn.

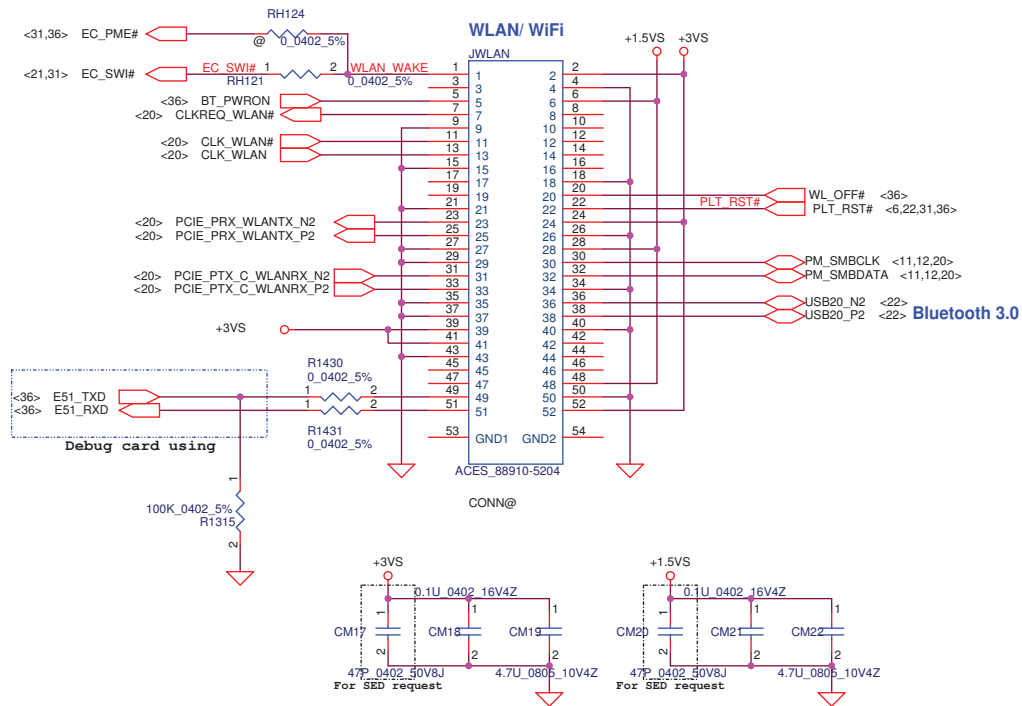


SATA ODD Conn

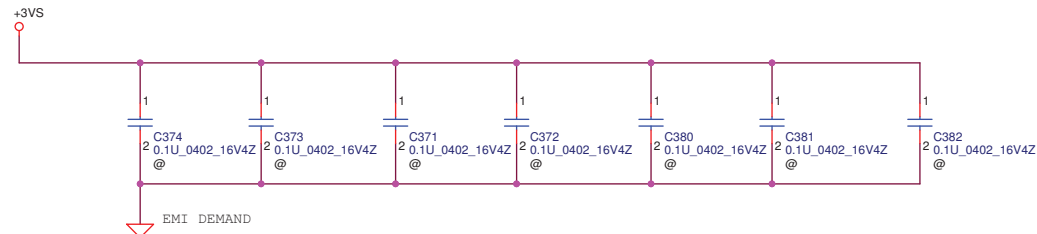
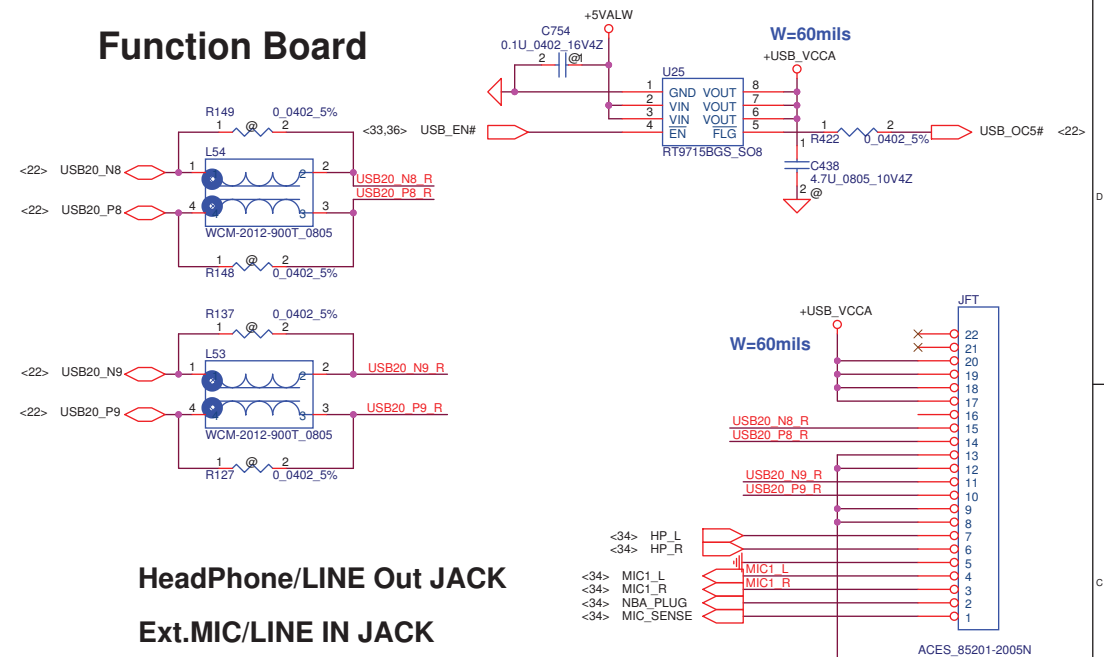


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Issued Date	2012/06/01	Deciphered Date	2013/05/12	SATA-HDD/ODD	
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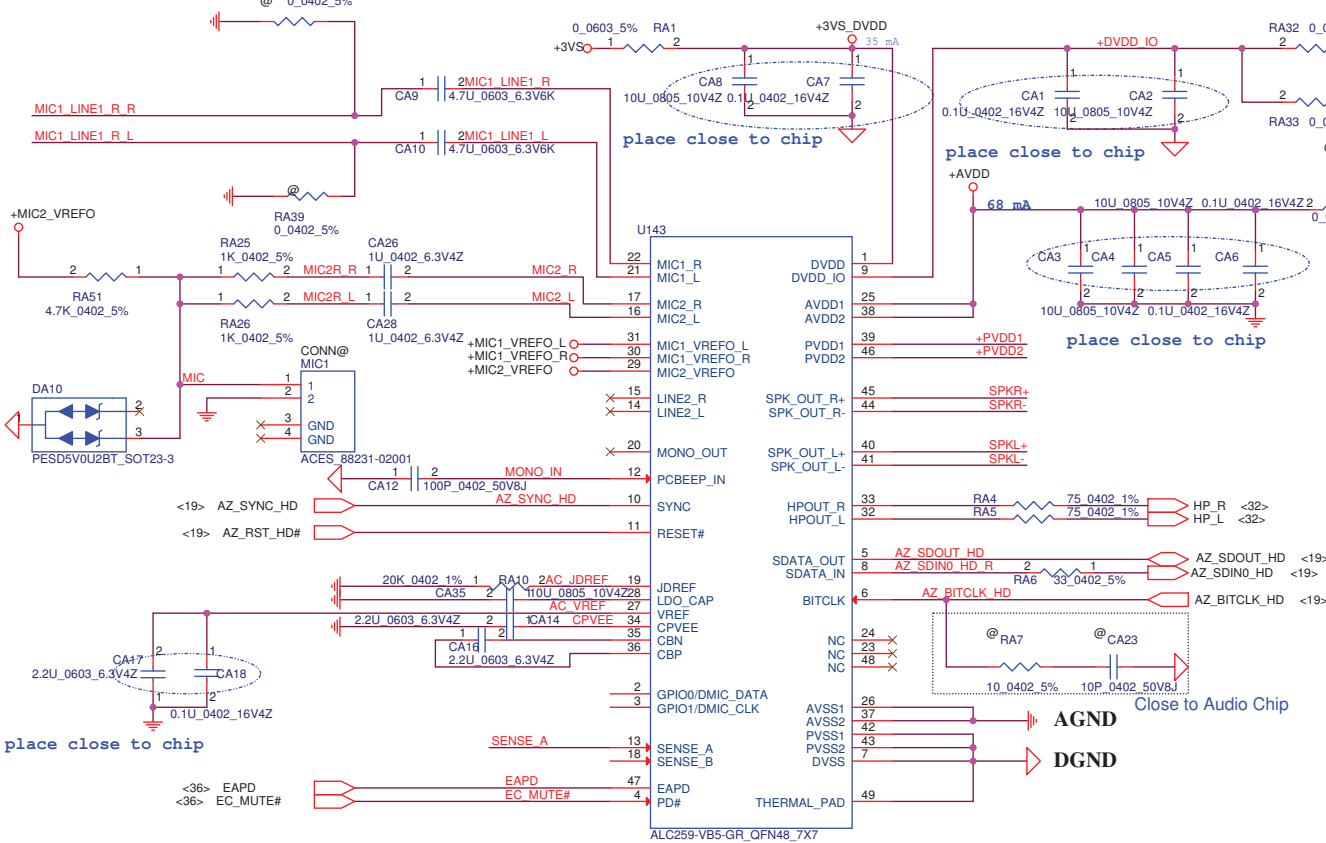
Slot 1 Half PCIe Mini Card-WLAN & BT3.0

Function Board

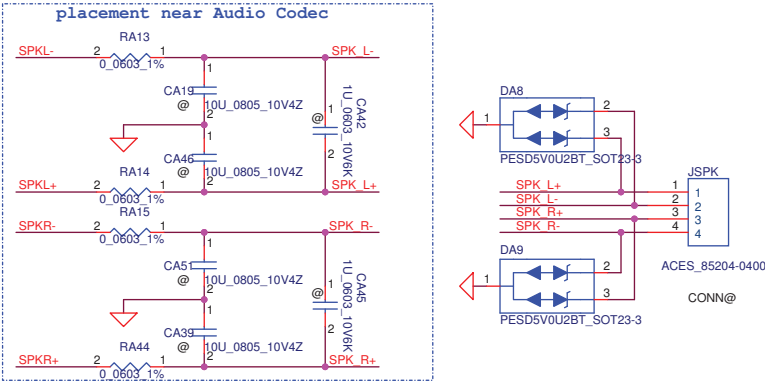


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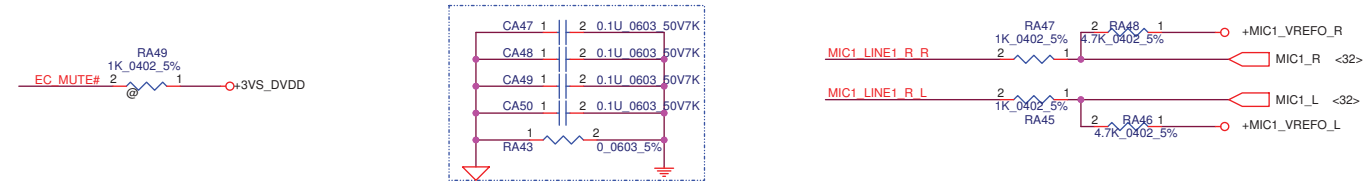
Ext. Mic/LINE IN



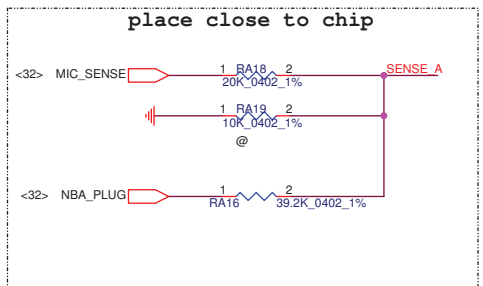
Speaker Connector



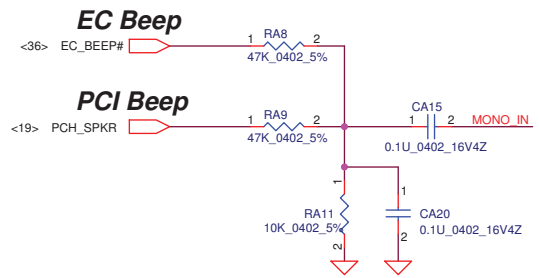
Ext.MIC/LINE IN JACK



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Ext. MIC
	20K	PORT-B (PIN 21, 22)	
	10K	PORT-C (PIN 23, 24)	SPK out
	5.1K	PORT-D (PIN 35, 36)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	Int. MIC
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 37)	Headphone out
	5.1K	PORT-I (PIN 32, 33)	

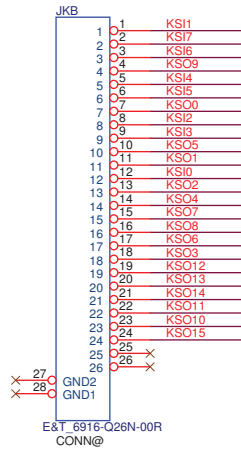


Beep sound



For EMC		
KSO10	1	2
C803	1	100P_0402_50V8J
KSO11	1	2
C804	1	100P_0402_50V8J
KSO12	1	2
C805	1	100P_0402_50V8J
KSO15	1	2
C807	1	100P_0402_50V8J
KSI7	1	2
C808	1	100P_0402_50V8J
KSI2	1	2
C810	1	100P_0402_50V8J
KSI3	1	2
C811	1	100P_0402_50V8J
KSI4	1	2
C812	1	100P_0402_50V8J
KSI0	1	2
C813	1	100P_0402_50V8J
KSI5	1	2
C814	1	100P_0402_50V8J
KSI6	1	2
C815	1	100P_0402_50V8J
KSI1	1	2
C816	1	100P_0402_50V8J
KSO2	1	2
C793	1	100P_0402_50V8J
KSO1	1	2
C790	1	100P_0402_50V8J
KSO4	1	2
C791	1	100P_0402_50V8J
KSO3	1	2
C792	1	100P_0402_50V8J
KSO5	1	2
C795	1	100P_0402_50V8J
KSO14	1	2
C796	1	100P_0402_50V8J
KSO6	1	2
C798	1	100P_0402_50V8J
KSO7	1	2
C799	1	100P_0402_50V8J
KSO13	1	2
C800	1	100P_0402_50V8J
KSO8	1	2
C801	1	100P_0402_50V8J
KSO9	1	2
C802	1	100P_0402_50V8J

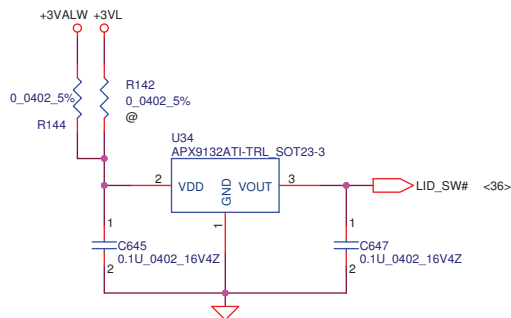
KEYBOARD CONN.



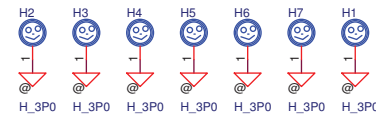
13.3" and 14"



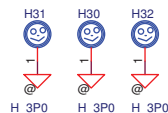
Lid SW



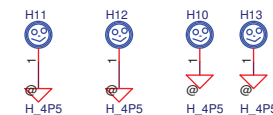
Screw Hole



Break hole



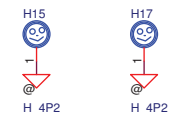
CPU



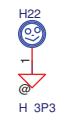
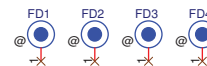
JWLAN



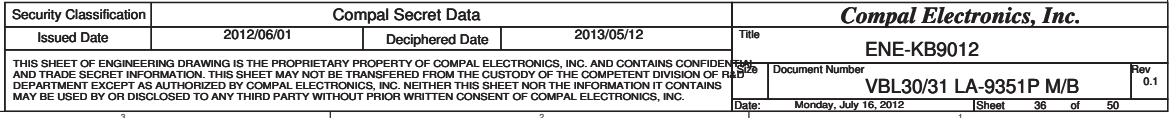
VGA



PCB Fedical Mark PAD



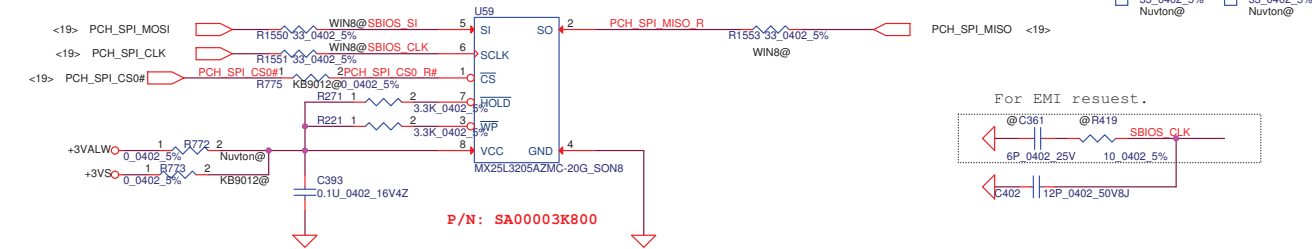
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	KB/PAD/ISPD/LID/ECROM
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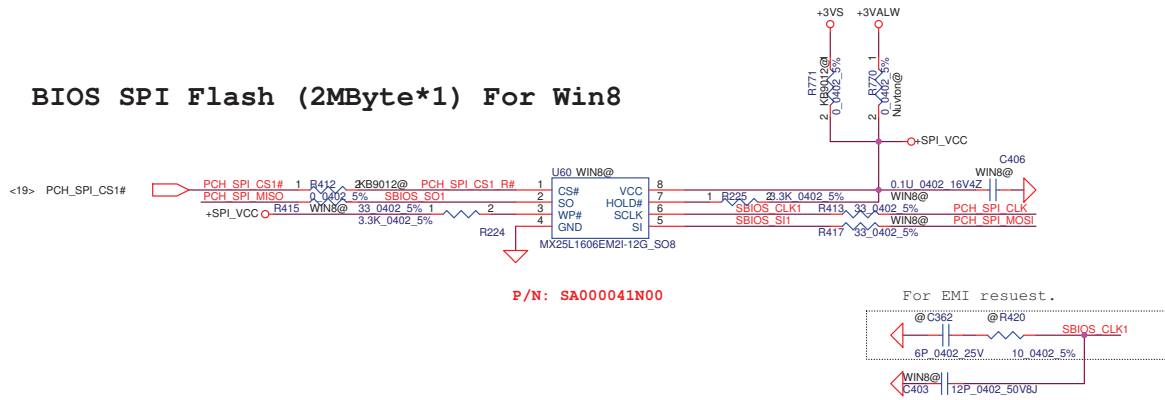
Pin	Signal	IO	Bank	Pin	Signal	IO	Bank
<36>	EC_SI_SPI_SO	Output	R266	1	Nuvoton@233	0402 5%	PCH SPI MISO R
<36>	EC_SO_SPI_SI	Input	R267	1	Nuvoton@233	0402 5%	SBIOS SI
<36>	SPI_CLK	Output	R271	1	Nuvoton@233	0402 5%	SBIOS CLK
<36>	SPI_CS#	Output	R270	1	Nuvoton@233	0402 5%	PCH SPI CS0 R#

When use single ROM, R1550 R1551 R1553use 0 ohm.

BIOS SPI Flash (4MByte*1)

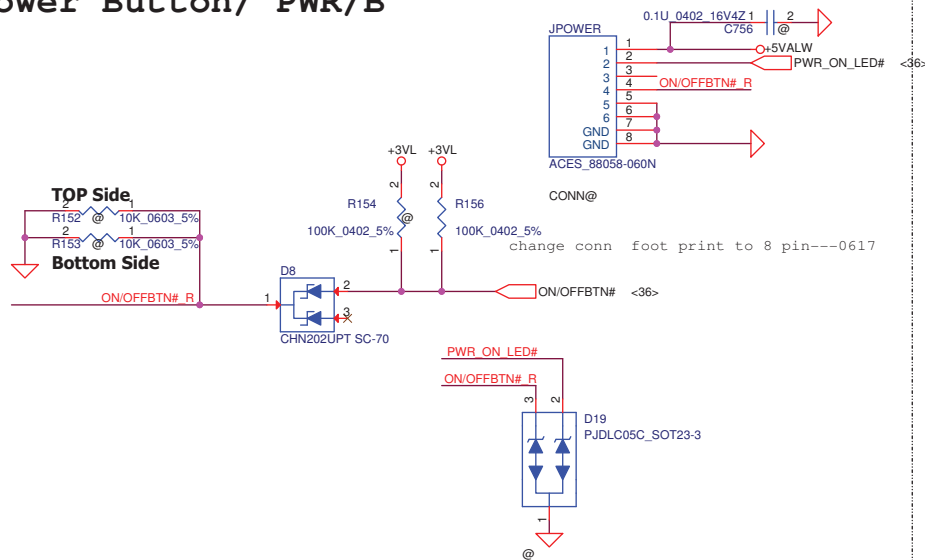


BIOS SPI Flash (2MByte*1) For Win8

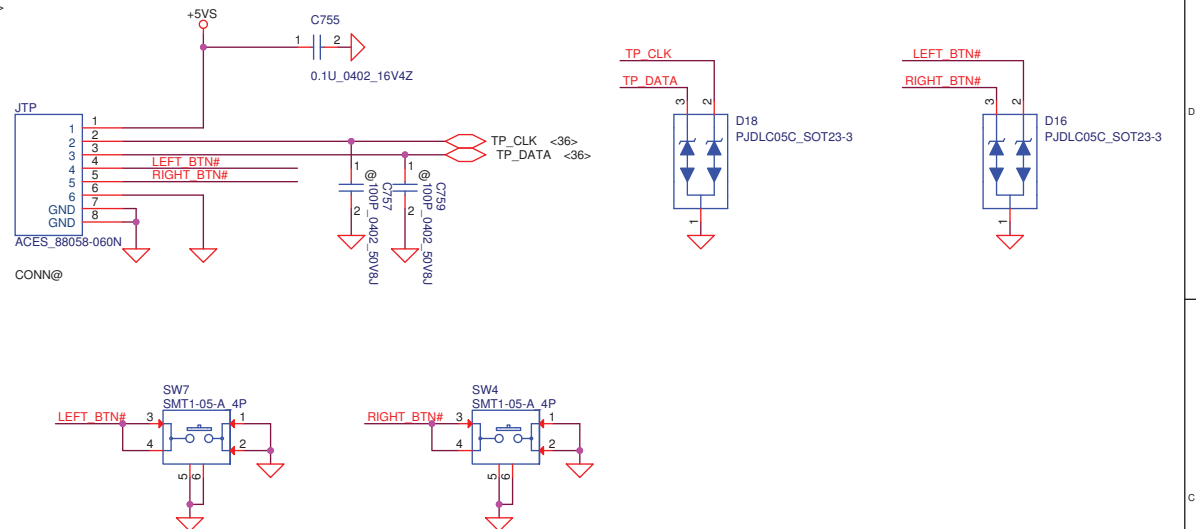


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Power Button/ PWR/B



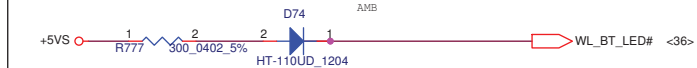
Touch/B Connector



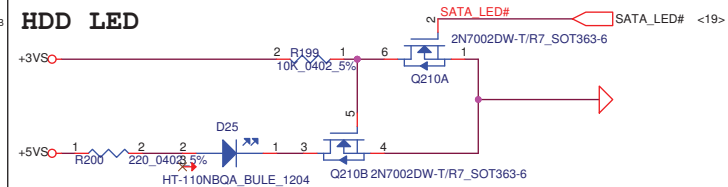
DC-IN LED



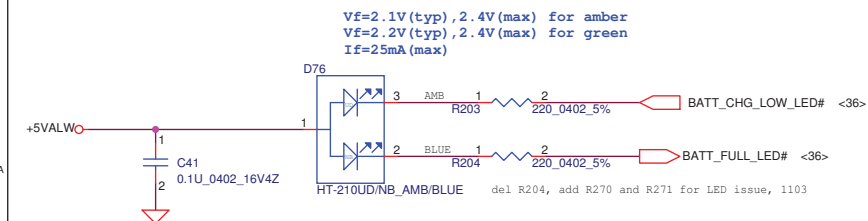
WL&BT LED



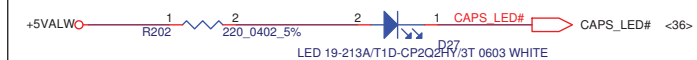
HDD LED



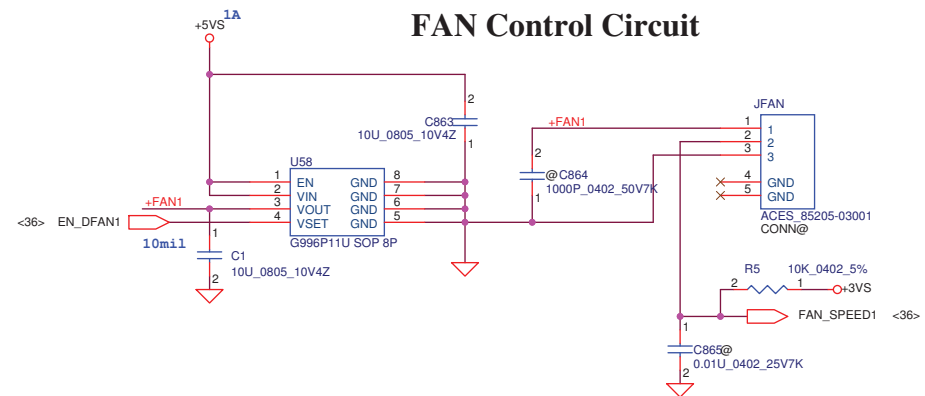
BATT CHARGE/FULL LED



CAP LOCK LED



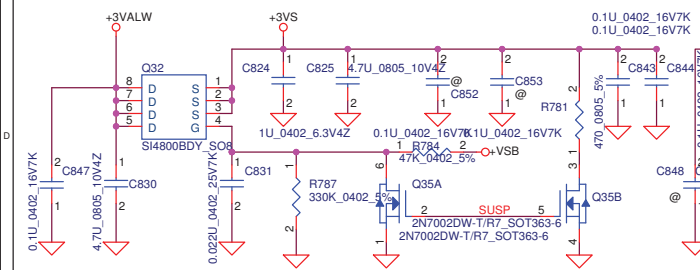
FAN Control Circuit



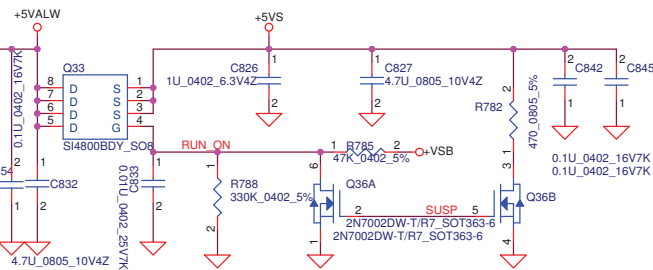
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+3VALW TO +3VS

Vgs=-0V, Id=9A, Rds=18.5mohm

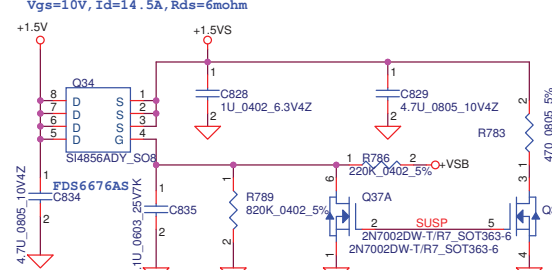


+5VALW TO +5VS

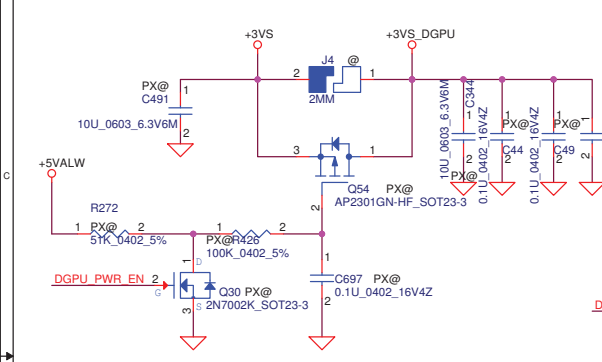


+1.5V TO +1.5VS

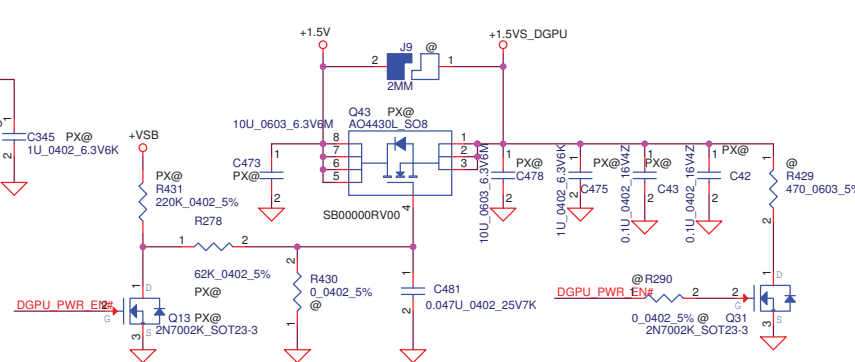
Vgs=10V, Id=14.5A, Rds=6mohm



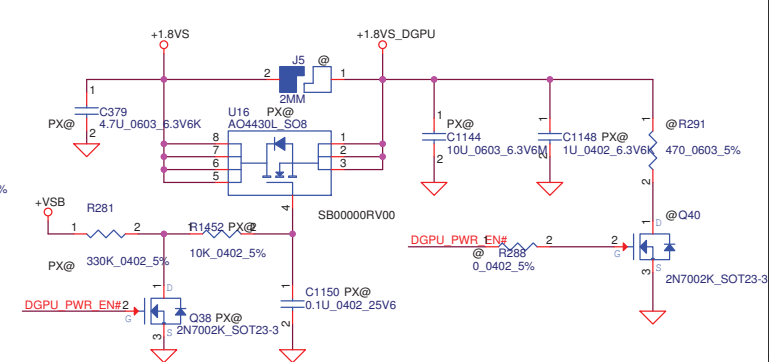
+3VS TO +3VS_DGPU



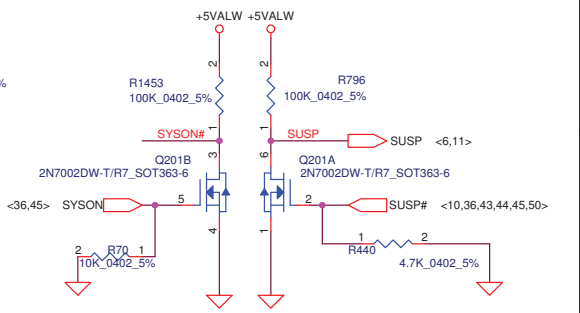
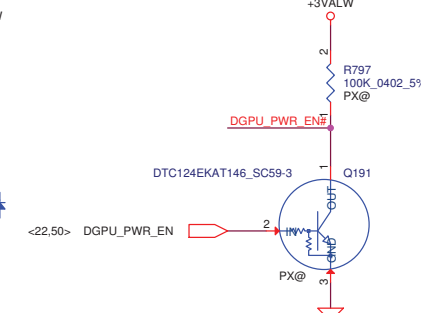
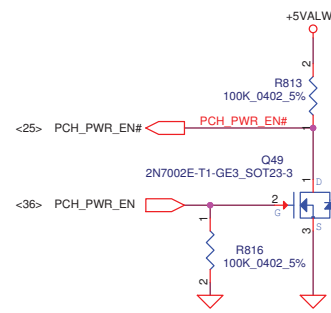
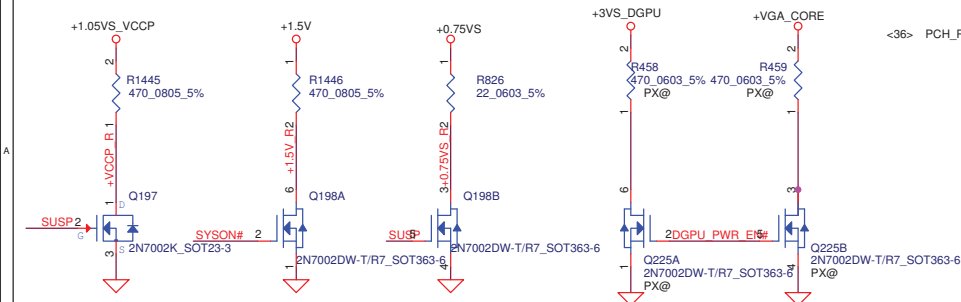
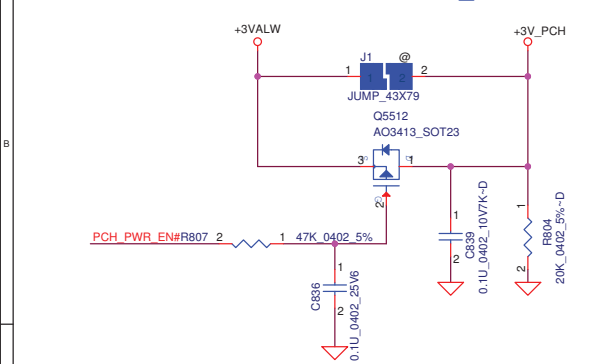
+1.5V TO +1.5VS_DGPU



+1.8VS TO +1.8VS_DGPU

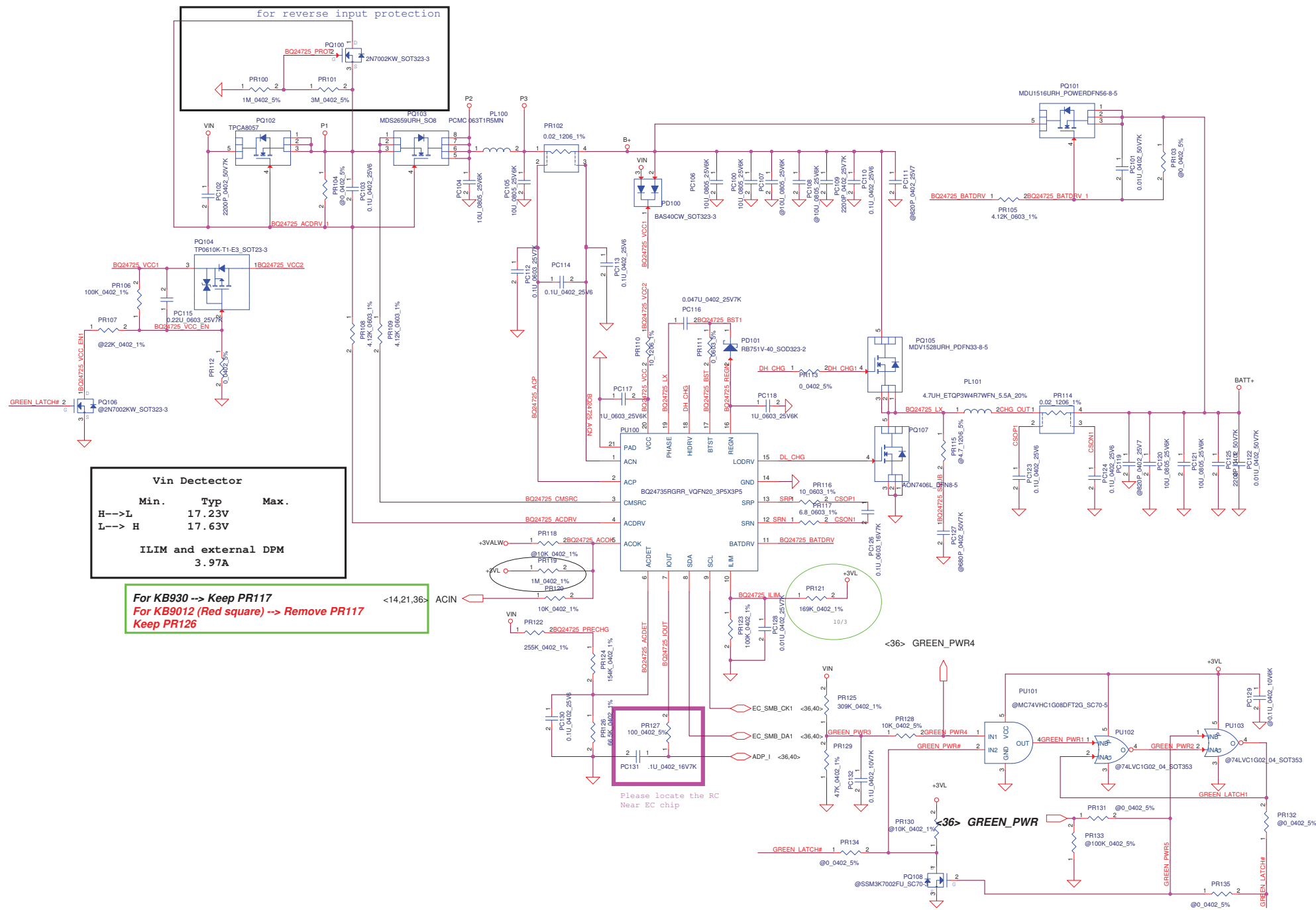


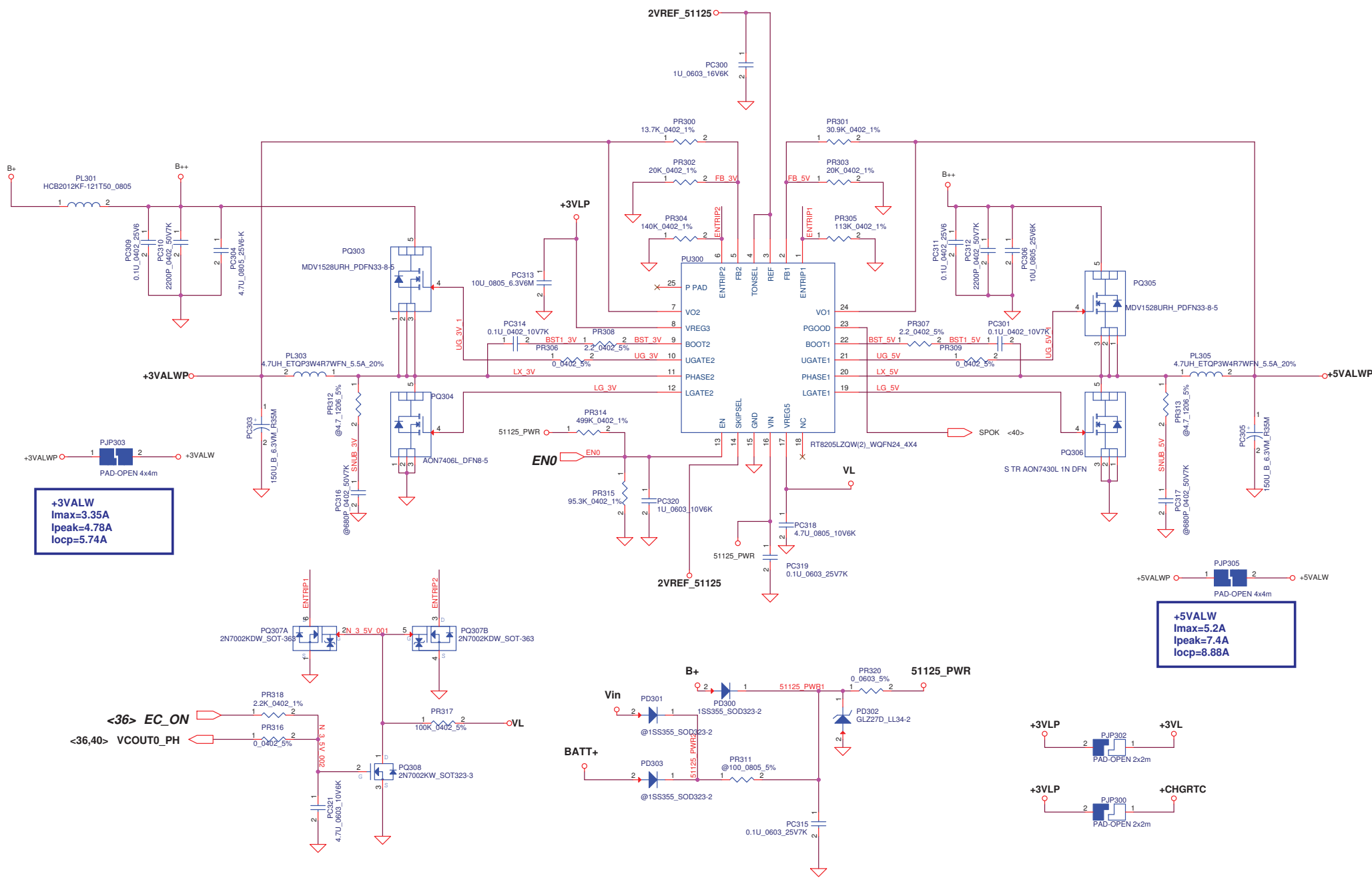
+3VALW to +3V_PCH



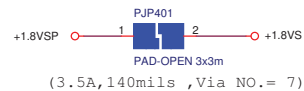
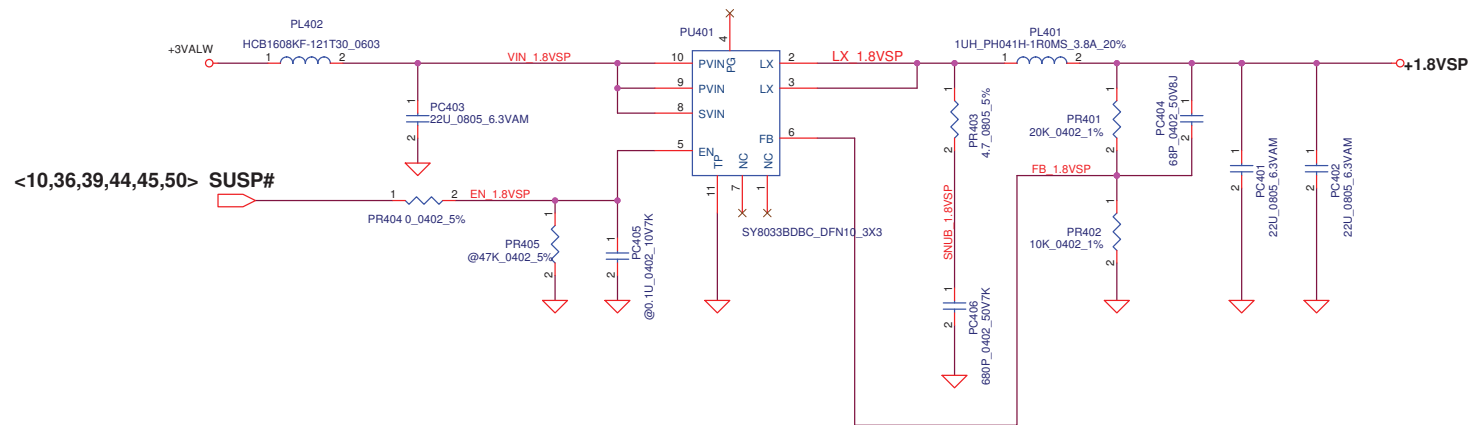
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Issued Date				2012/06/01				Deciphered Date			
2012/06/01				2013/05/12				Title			
2013/05/12				DC-DC INTERFACE				Document Number			
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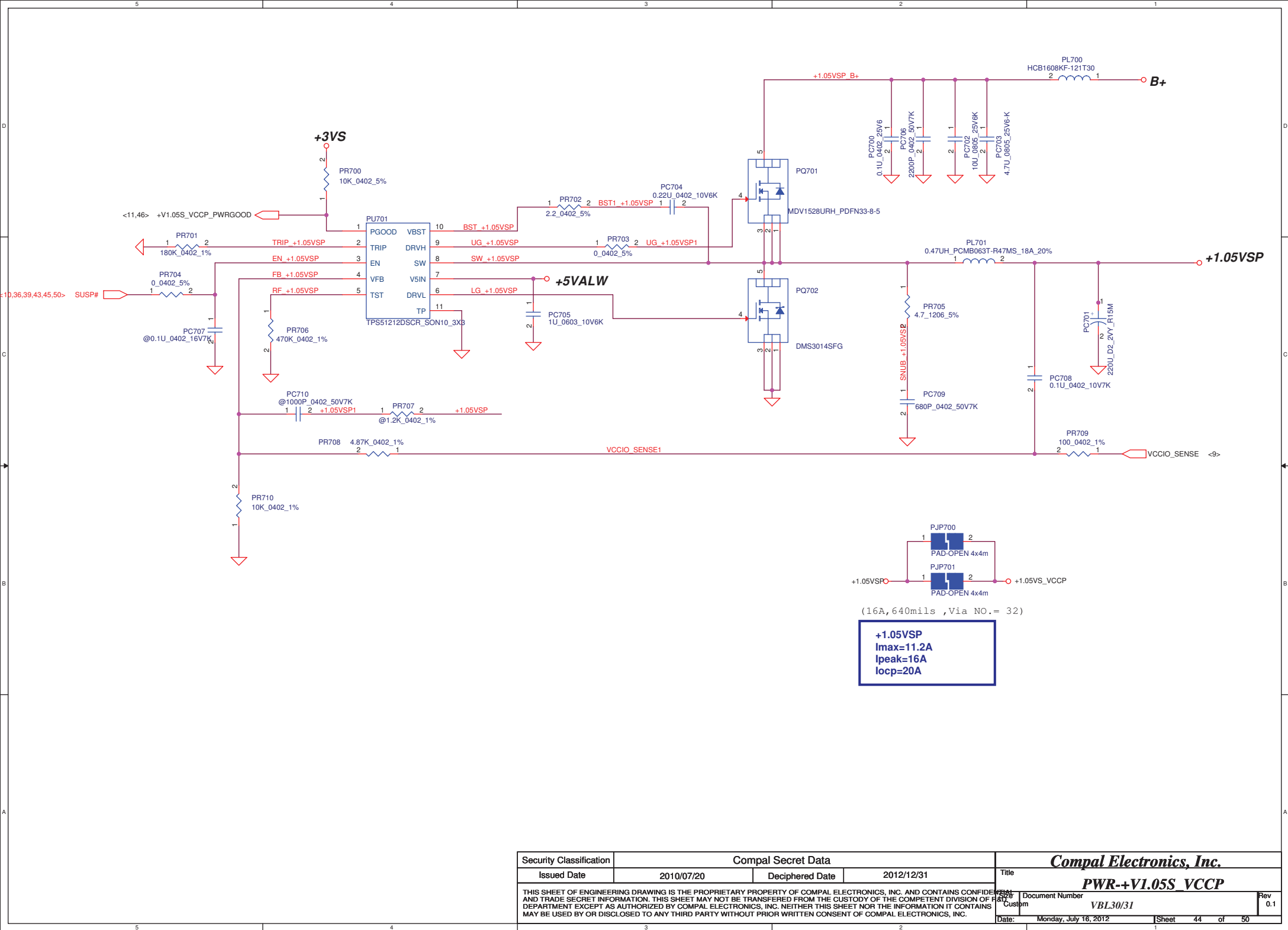




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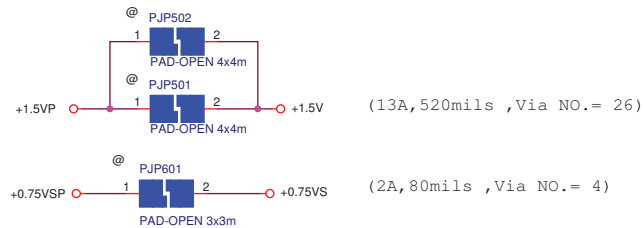


+1.8V
I_{max}=2.25A
I_{peak}=3.22A



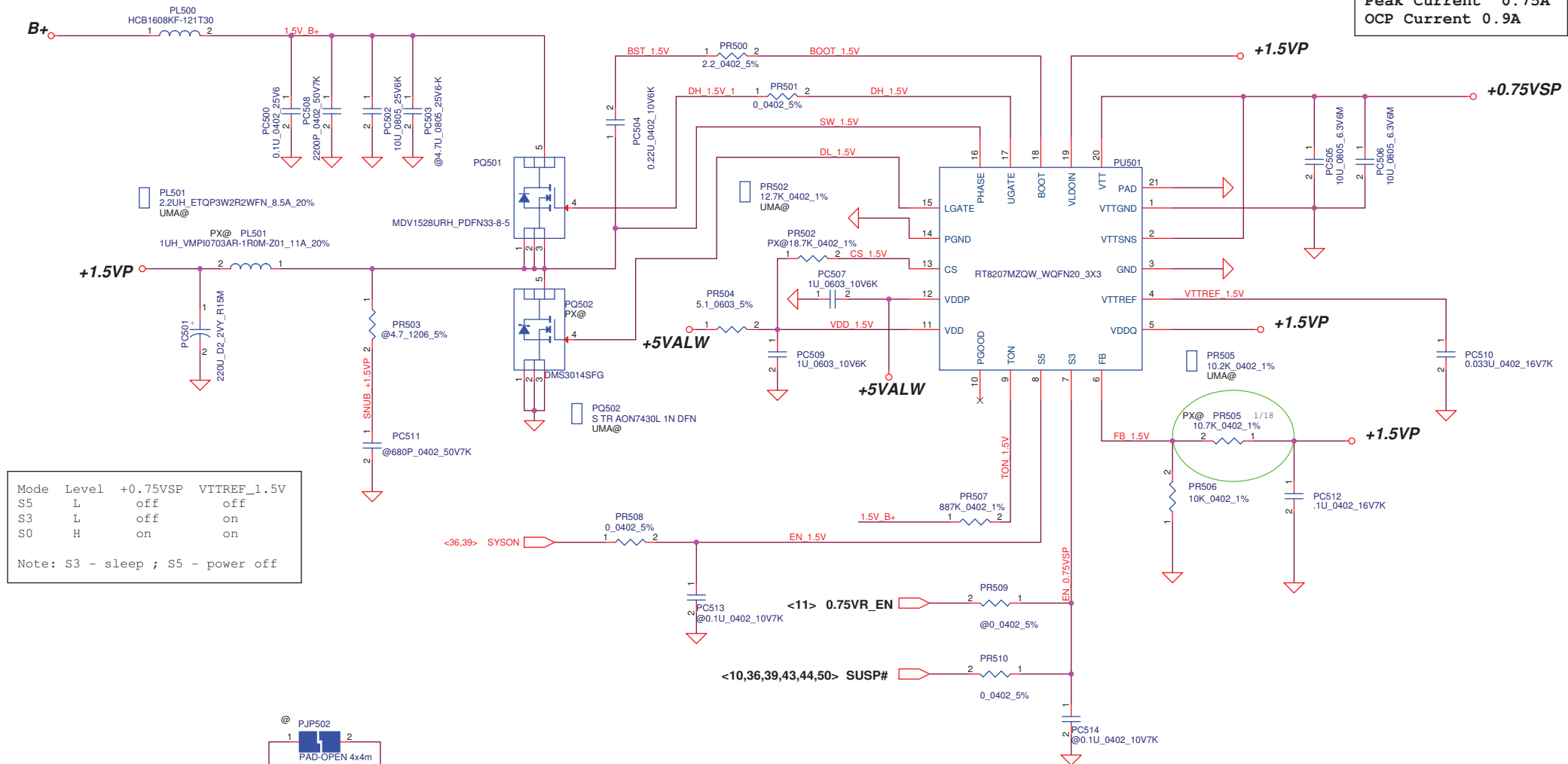
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				Rev	0.1

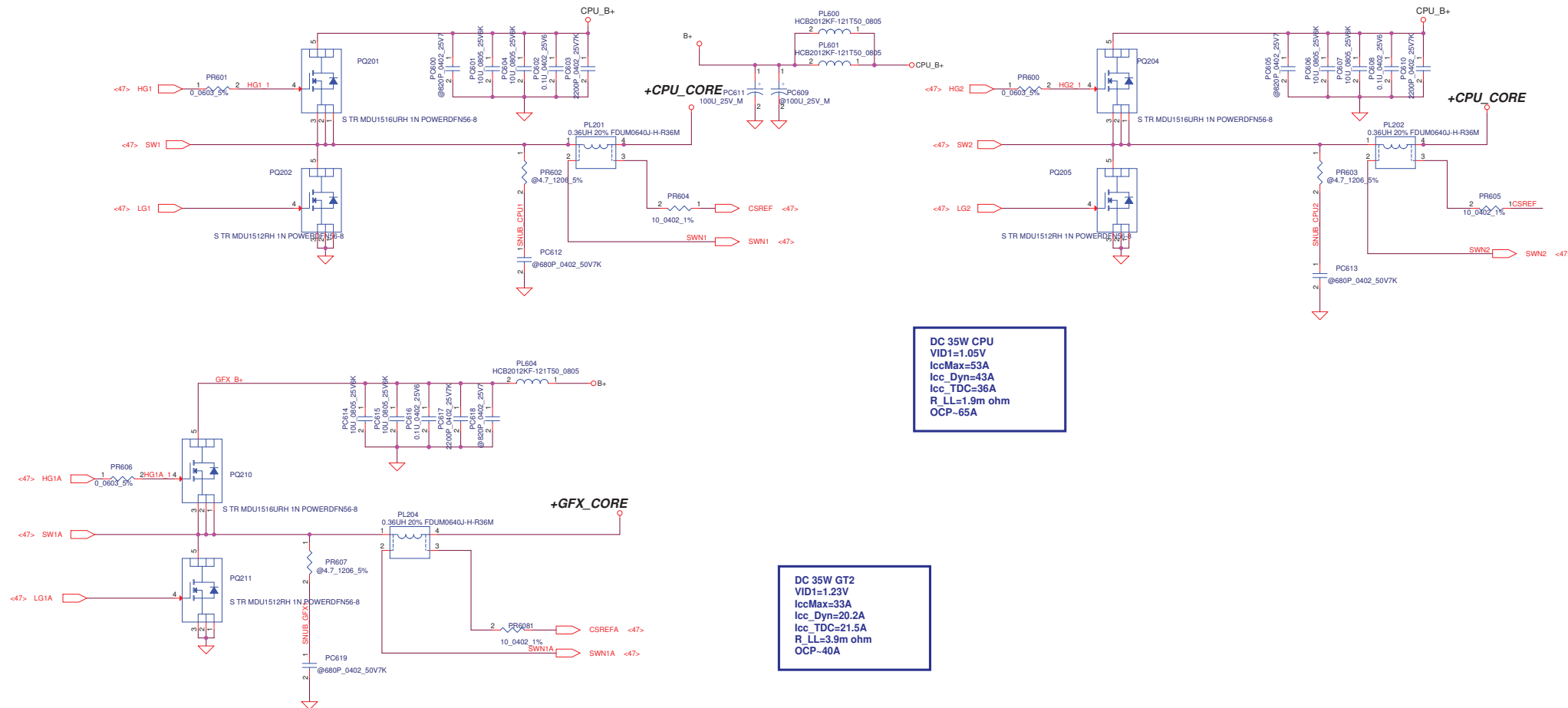
Mode Level +0.75VSP VTTREF_1.5V
S5 L off off
S3 L off on
S0 H on on
Note: S3 - sleep ; S5 - power off



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0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A



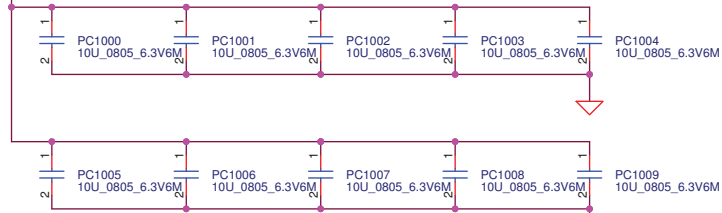


DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP=65A

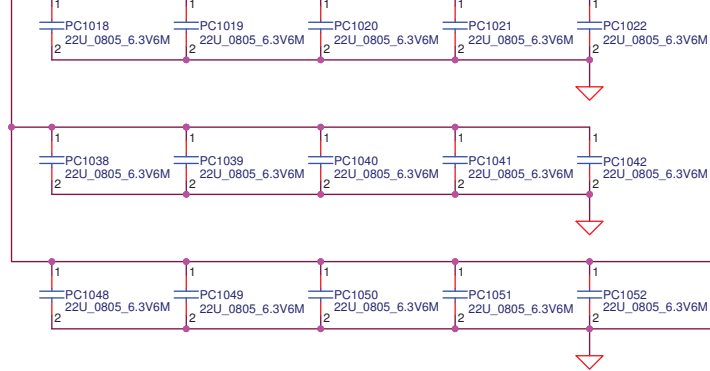
DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP=40A

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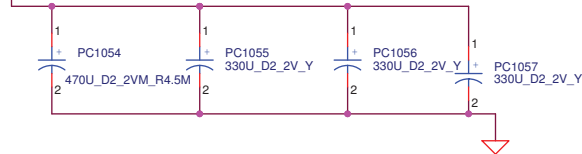
+CPU_CORE



+CPU_CORE



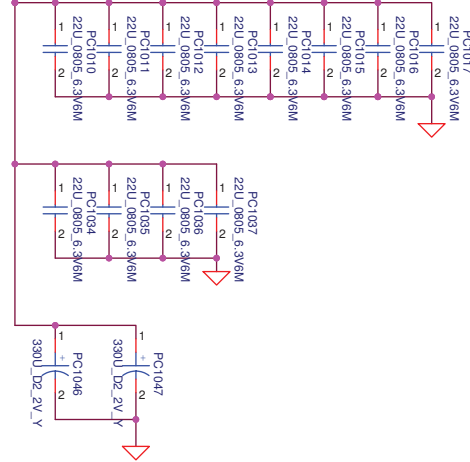
+CPU_CORE



+CPU_CORE

+GFX_CORE

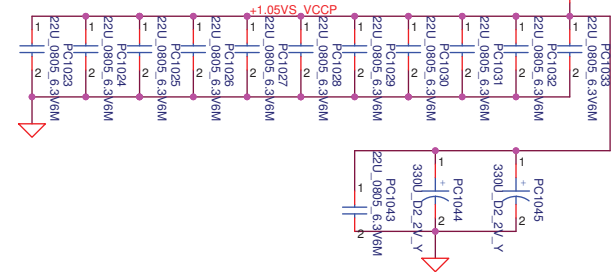
+GFX_CORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

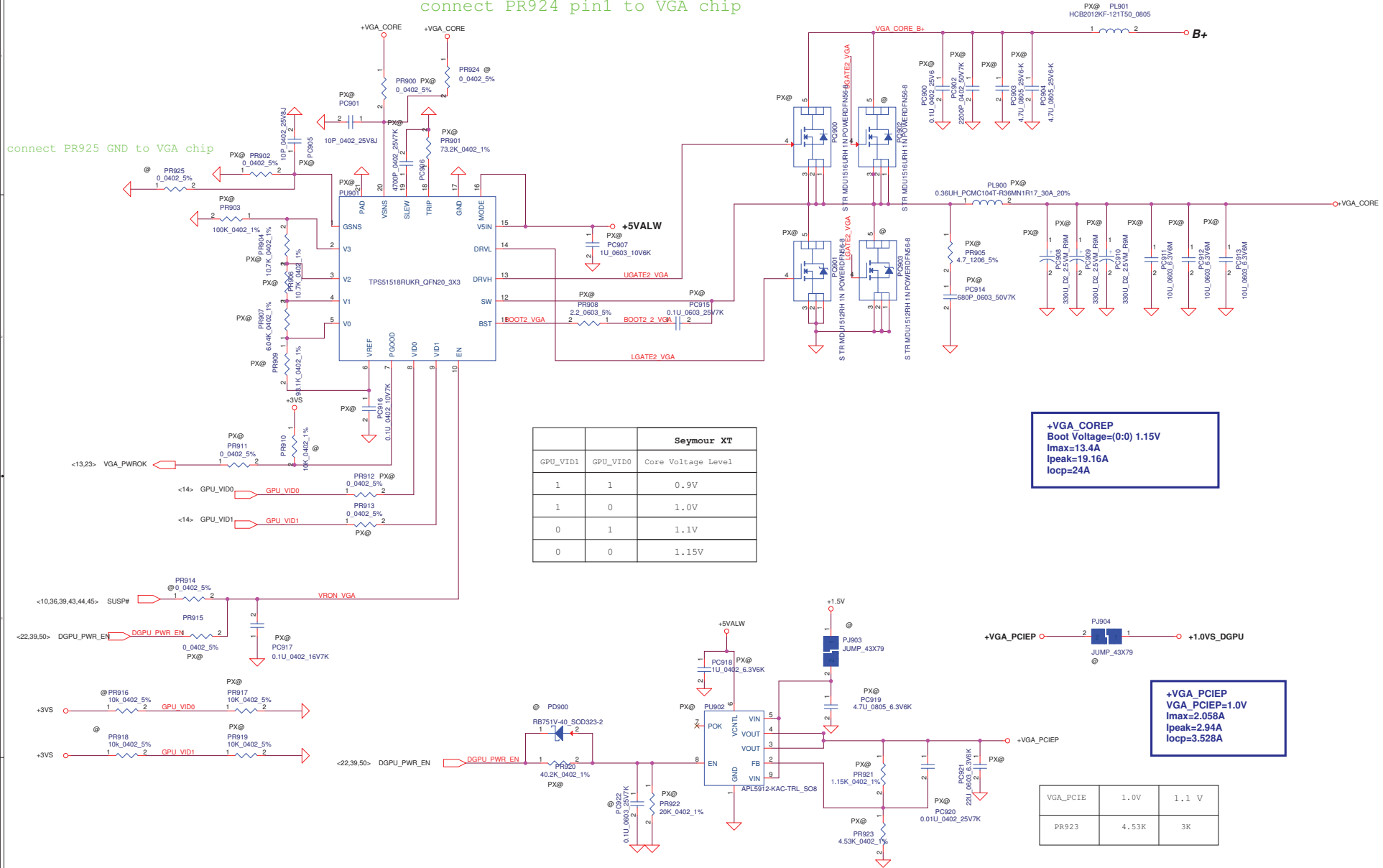
+1.05VS_VCCP



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connect PR924 pin1 to VGA chip

connect PR925 GND to VGA chip



Seymour XT		
GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V
1	0	1.0V
0	1	1.1V
0	0	1.15V

+VGA_CORE
Boot Voltage=(0:0) 1.15V
Imax=13.4A
Ipeak=19.16A
Iocp=24A

+VGA_PCIEP
VGA_PCIEP=1.0V
Imax=2.058A
Ipeak=2.94A
Iocp=3.528A

VGA_PCIE	1.0V	1.1 V
PR923	4.53K	3K

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